EXHIBIT 1

Sreenivasan, Priya

From: Sreenivasan, Priya
Sent: Monday, November 12, 2007 4:55 PM
To: 'hdoscher@morganlewis.com'; awu@morganlewis.com
Cc: bschuman@morganlewis.com; aspicer@morganlewis.com; rtautkus@morganlewis.com; rwilkins@morganlewis.com; ahoffman@morganlewis.com; Jacobs, Eric P.; Shoiket, Igor; Hulse, Matthew R; Augustine Jr., Leonard J.
Subject: Fairchild/AOS: Today's Meet and Confer

Dear Andrew and Harry:

This e-mail serves to memorialize our telephone conference that occurred at 3 p.m. today (11/12). In the first part of the teleconference, Eric Jacobs again raised the issue of both parties agreeing to provide discovery on representative parts. Eric's reasoning was that it would reduce the costs of discovery, litigation and eventually, those representative parts would be litigated at trial. Eric also suggested that each party could verify the opposing party's representative parts list through: 1) an interrogatory response that identifies the relevant manufacturing documents and which parts they represent and/or 2) a 30(b)(6) deposition regarding representative parts and/or 3) each party can send the opposing party a list of the parts that are representative in each category and the opposing party can randomly choose an agreed number of parts for which to obtain discovery. Andrew stated that the main concern for AOS was: 1) parts may be left off the list and 2) whether the parts are truly representative. Eric suggested that each party could take an early 30(b)(6) deposition to ensure that the parts are truly representative. Eric also suggested that this would save money and reduce discovery obligations and that this type of "representative parts" agreement has been in every semiconductor case that he has litigated. Eric further suggested that Andrew ask his client about the types of documents that AOS needs to prove its infringement case and to identify those specific documents for Fairchild. Andrew stated that he will talk to his team and his client and determine whether he can agree to the above issues.

The second part of the telephone conference was directed to AOS's new definition of "Accused Fairchild Devices" which was defined in the November 8, 2007, letter from Harry Doscher to Priya Sreenivasan. Eric raised the issue of whether the word "including" in the introduction of the definition was intended to be an open-ended "including without limitation." Andrew answered that they did not mean to say "without limitation" and that the list of items was complete. Eric stated that he wanted to make sure that the definition included a device made, used, sold, offered for sale or imported by Fairchild in the United States. Andrew stated that he was not sure if the parts had to be imported in the United States by Fairchild, as opposed to a customer. Eric stated that Fairchild needed to think about that definition. Eric asked Andrew what is a "power MOSFET-based" device. Andrew explained that it is any integrated circuit that includes a power MOSFET. Eric then stated that part (a) of AOS's new definition was too broad and covered far more than the '567 patent claims. David Schnapf of Townsend stated that the essential feature of the '567 patent is that you have subcontact areas and the subcontact areas have more than one lead wire. Andrew stated that if Fairchild has an alternative definition for part (a) of AOS's new definition, AOS would be willing to consider it. We agreed to provide AOS with an alternative definition to part (a). For part (b), David stated that the definition was also too broad and that we will provide another proposed definition for part (b). For part (c), David stated that the '630 patent requires 3 dopant implants into a body region. David further stated that if the definition for part (c) was changed from 2 body dopant implants to 3 body dopant implants, the definition would be acceptable to Fairchild. David stated that part (d) of AOS's new definition was overbroad so as to include any other device identified by AOS. Andrew stated that they had included part (d) as a part of their original discovery requests because they thought new patents may be added later and that at this point, AOS will consider whether it is still necessary to have part (d) of AOS's new definition. Finally, David stated that there should be an "and/or" between parts (b) and (c) of AOS's new definition.

Fairchild has agreed to provide AOS with a new definition of "Accused Fairchild Device" by tomorrow (11/13) at noon. Both parties have tentatively agreed to have a teleconference tomorrow at 2 p.m. to discuss the definition further.

Please let me know if this does not accurately reflect our discussion.

Regards,

Priya Sreenivasan, Esq.
Litigation Associate
Townsend and Townsend and Crew, LLP
Two Embarcadero Center, 8th Floor

San Francisco, CA 94111
Phone: 415.273.4742
Fax: 415.576.0300
psreenivasan@townsend.com
www.townsend.com

EXHIBIT 2

Sreenivasan, Priya

From: Sreenivasan, Priya
Sent: Tuesday, November 13, 2007 4:08 PM
To: 'hdoscher@morganlewis.com'
Cc: Ahren C. Hoffman; Amy M. Spicer; Andrew J. Wu; bschuman@morganlewis.com; Rita E. Tautkus; R. Wilkins; Jacobs, Eric P.; Shoiket, Igor; Hulse, Matthew R; Augustine Jr., Leonard J.
Subject: 11/13/07 Telephonic Meet and Confer

Dear Harry:

This e-mail serves to memorialize our 2 p.m. phone call today (11/13) regarding Fairchild's proposed definition of "Accused Fairchild Devices." On that call, you were the only Morgan Lewis lawyer who participated (as opposed to the five Townsend lawyers who were prepared to discuss Fairchild's proposed definition, which was the purpose of the call). You stated in the phone call that it is AOS's position that Fairchild's proposed definition of "accused devices" sent to you today was too narrow. However, when we asked why the definition proposed by Fairchild was too narrow, you were unable to explain or articulate an answer (other than to state that AOS was entitled to all information reasonably calculated to lead to the discovery of admissible evidence). You further indicated that the meet and confer process had gone on too long and that AOS needed to "proceed to the next step." When I asked you about whether Morgan Lewis had spoken to AOS regarding the representative parts agreement raised by Eric Jacobs in the 11/12 telephonic meet and confer, you were not prepared to discuss the issue.

Regards,

Priya Sreenivasan, Esq.
Litigation Associate
Townsend and Townsend and Crew, LLP
Two Embarcadero Center, 8th Floor
San Francisco, CA 94111
Phone: 415.273.4742
Fax: 415.576.0300
psreenivasan@townsend.com
www.townsend.com

Offices in: Denver | Palo Alto | San Diego | San Francisco | Seattle | Tokyo | Walnut Creek | Washington D.C.

EXHIBIT 3

US005767567A

United States Patent [19]

Hu et al.

[11] Patent Number: 5,767,567

[45] Date of Patent: Jun. 16, 1998

[54] **DESIGN OF DEVICE LAYOUT FOR INTEGRATION WITH POWER MOSFET PACKAGING TO ACHIEVE BETTER LEAD WIRE CONNECTIONS AND LOWER ON RESISTANCE**

[75] Inventors: **Yung-Chang Hu**; **Tsuo-Hsin Ma**, both of Taipei, Taiwan

[73] Assignee: **MageMos Corporation**, Taipei, Taiwan

[21] Appl. No.: **707,929**

[22] Filed: **Sep. 10, 1996**

[51] **Int. Cl.**[6] **H01L 23/495**

[52] **U.S. Cl.** **257/666**; 257/401

[58] **Field of Search** 257/401, 412, 257/330, 331, 153, 249, 666; 438/618, 617, 123

[56] **References Cited**

U.S. PATENT DOCUMENTS

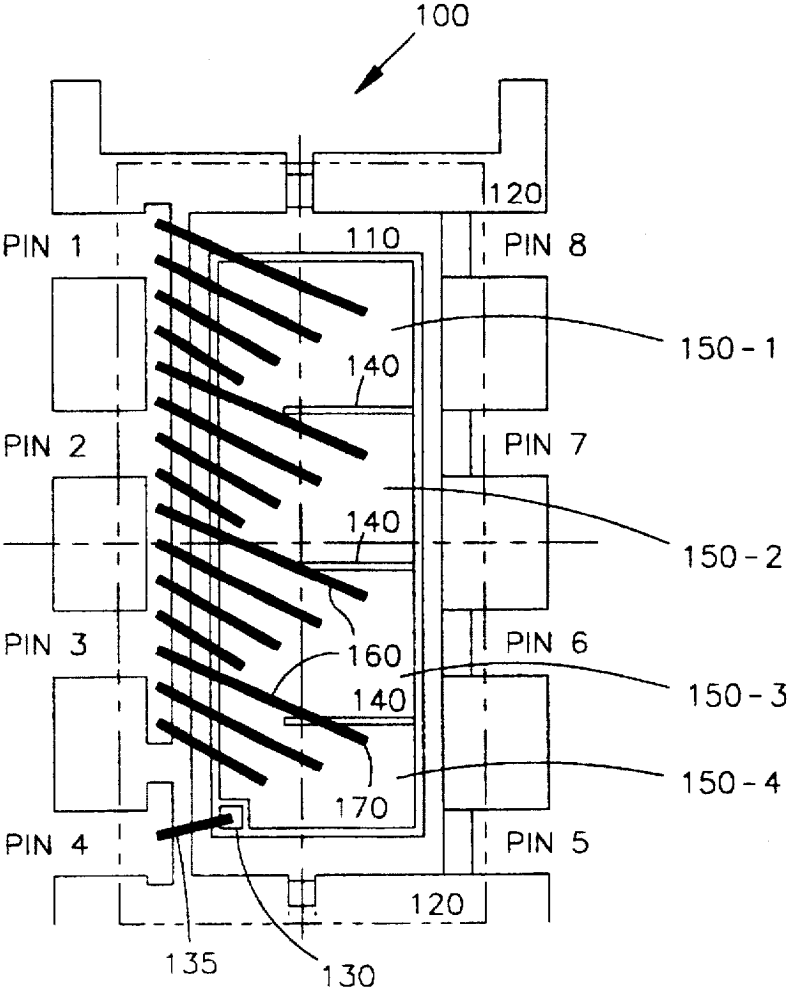
5,306,937 4/1994 Nishimura .
5,497,013 3/1996 Temple .
5,544,038 8/1996 Fisher et al. .
5,661,315 8/1997 Bauer et al. .

Primary Examiner—Mahshid D. Saadat
Assistant Examiner—S. V. Clark
Attorney, Agent, or Firm—Bo-In Lin

[57] **ABSTRACT**

The present invention discloses a MOSFET power IC device formed in a semiconductor chip including a source contact area which is provided for connecting to a lead-frame via a several of lead-wires. The power IC device includes many lead-wire contact points on the source contact area for securely attaching the lead wires onto the source contact area. These lead-wire contact points are uniformly distributed substantially over the source contact area thus the spread resistance is reduced whereby the device on-resistance and device performance may be improved.

8 Claims, 7 Drawing Sheets



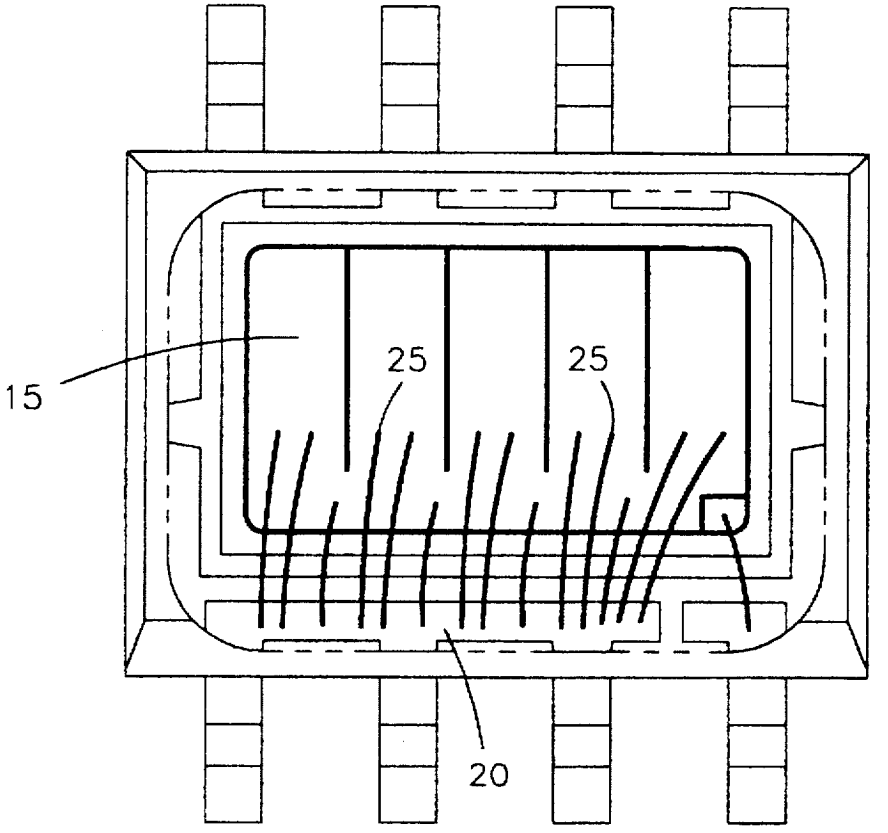


FIG. 1A
(PRIOR ART)

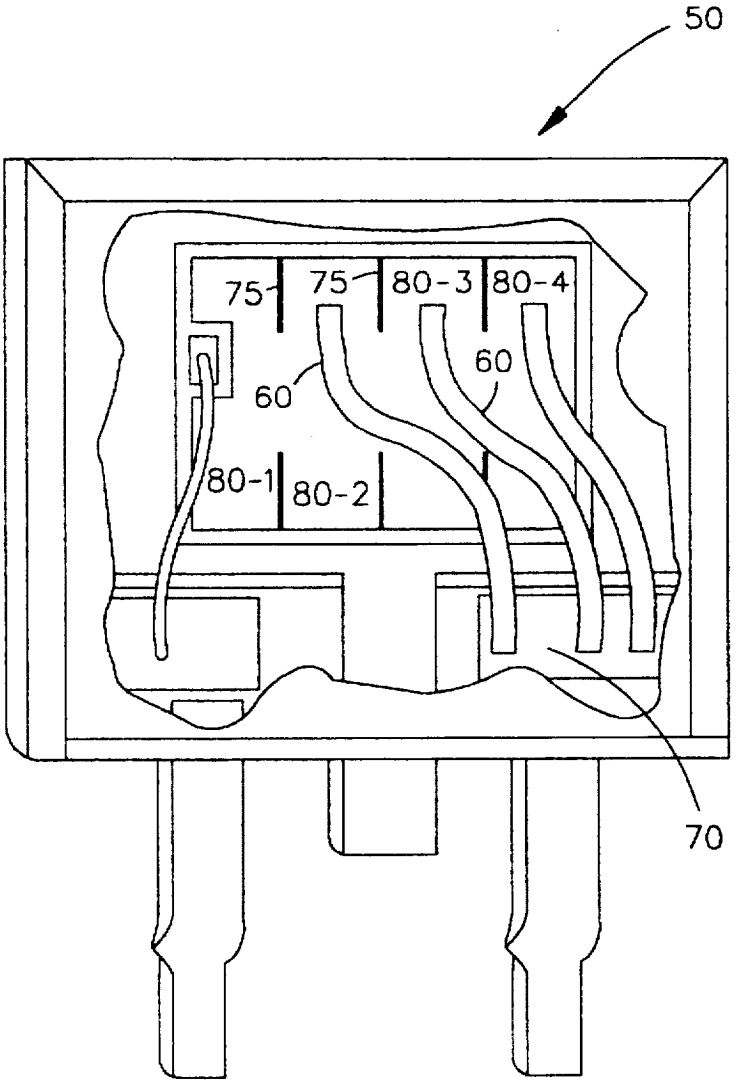


FIG. 1B
(PRIOR ART)

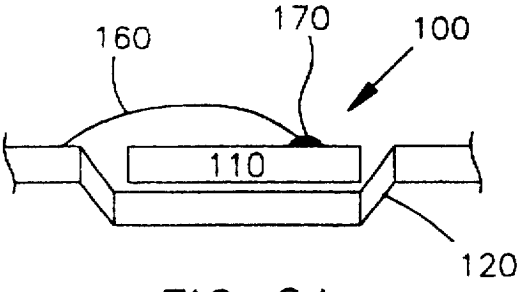

160
170
100
110
120

FIG. 2A

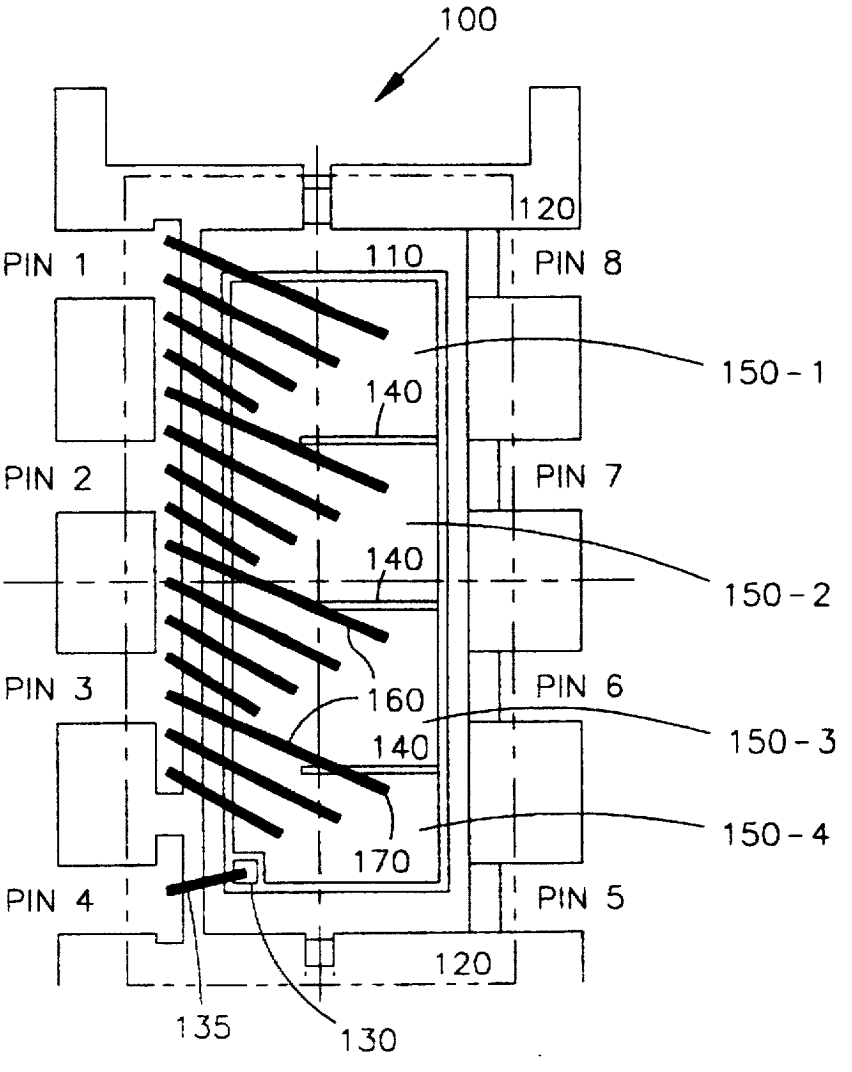

100
120
PIN 1
110
PIN 8
150-1
140
PIN 2
PIN 7
140
150-2
PIN 3
160
PIN 6
140
150-3
150-4
170
PIN 4
PIN 5
120
135
130

FIG. 2B

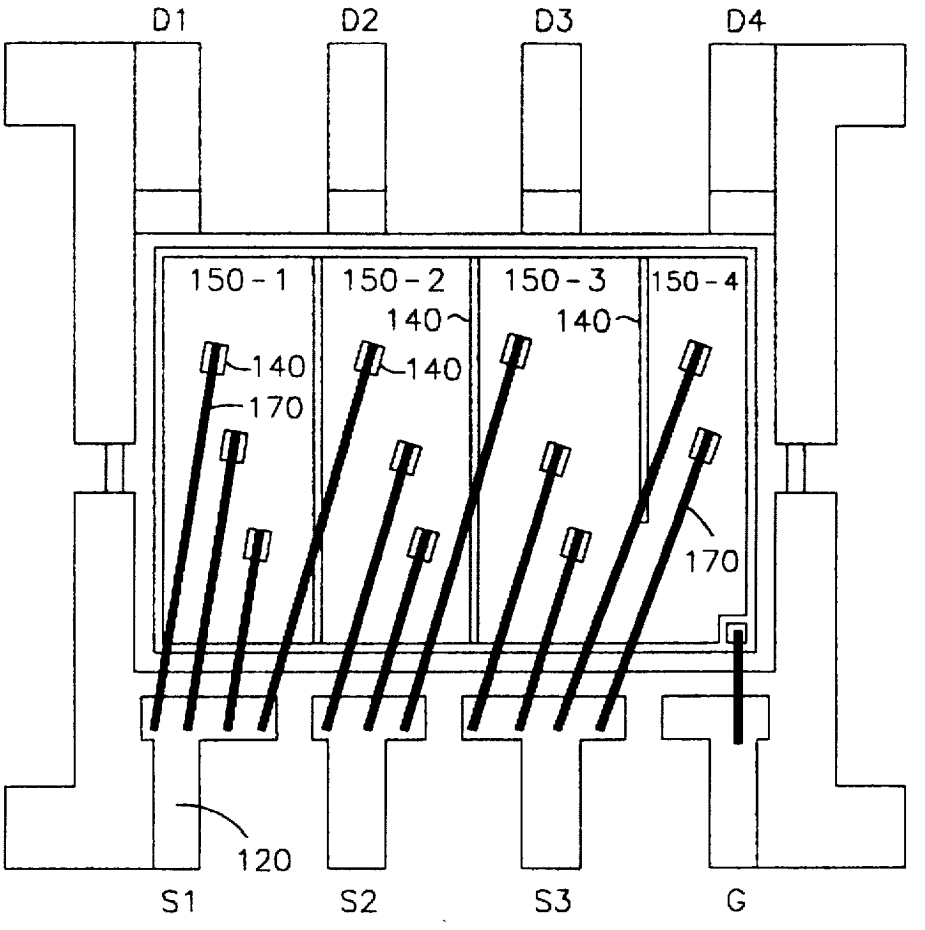

D1
D2
D3
D4
150-1
150-2
150-3
150-4
140
140
140
140
170
170
120
S1
S2
S3
G

FIG. 2C

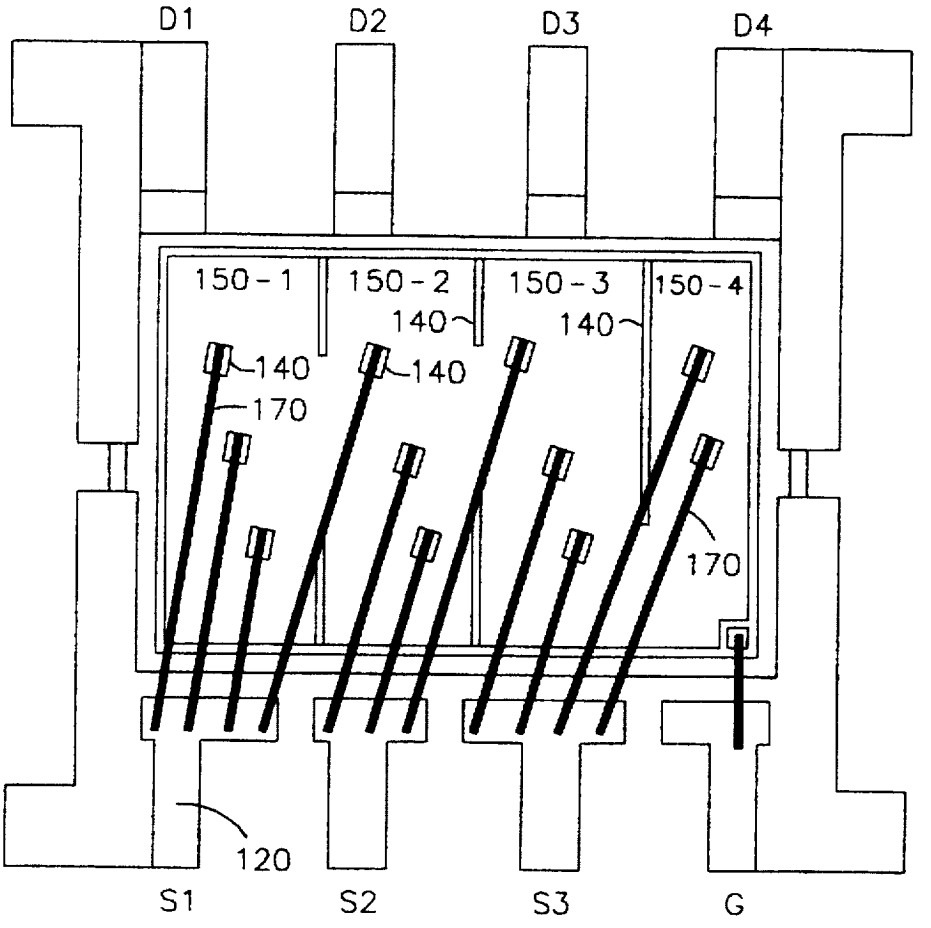

D1
D2
D3
D4
150-1
150-2
150-3
150-4
140
140
140
140
170
170
120
S1
S2
S3
G

FIG. 2D

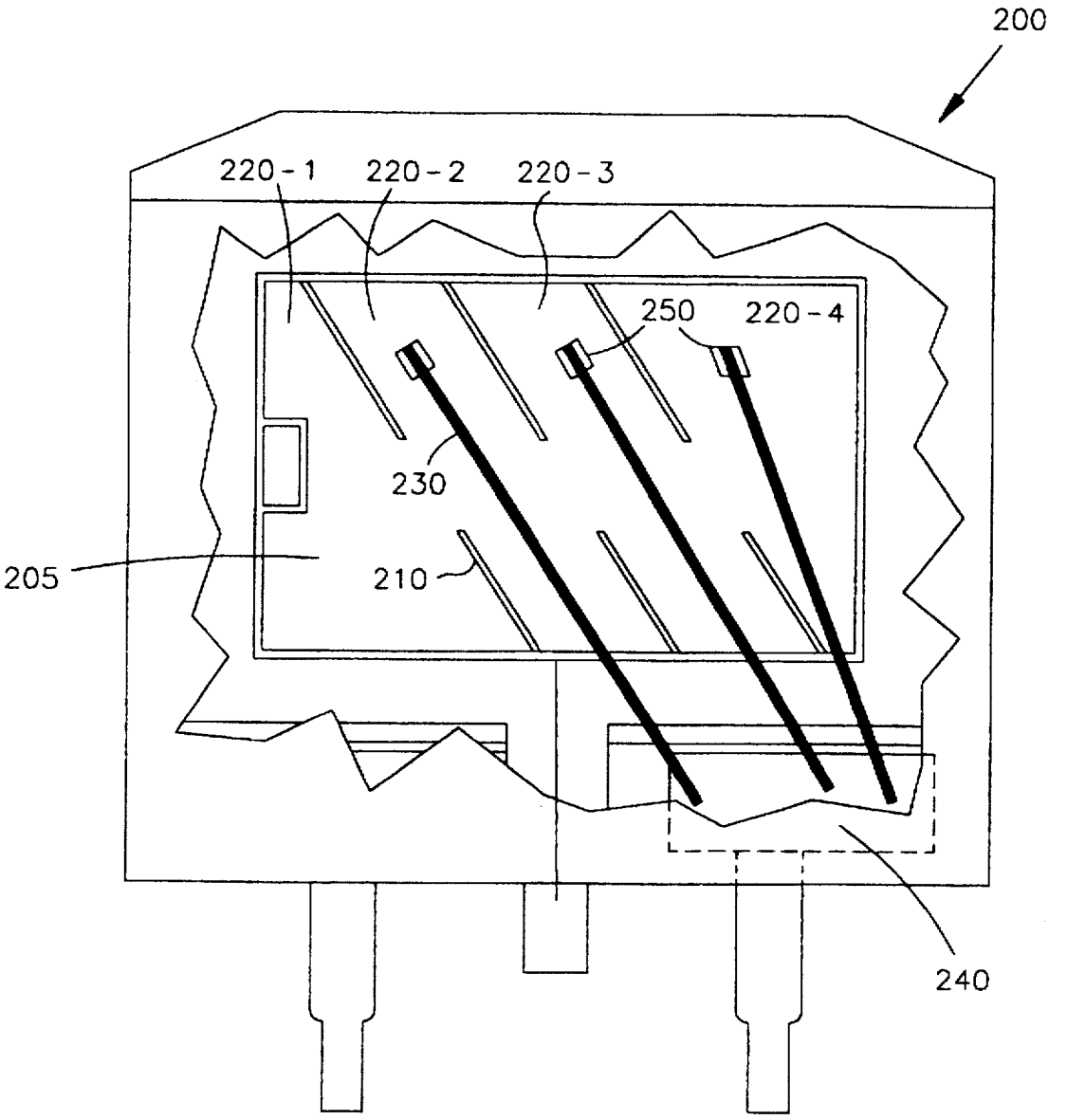


FIG. 3

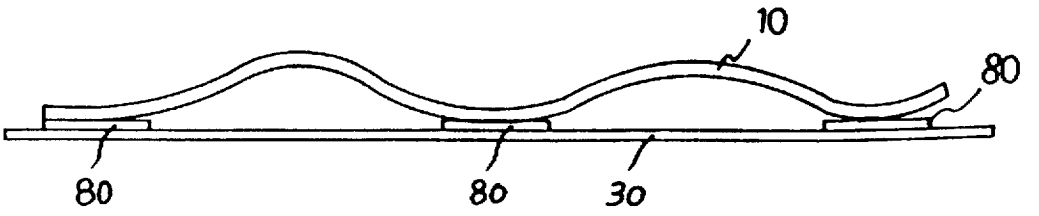

10
80
80
80
30

FIG. 4

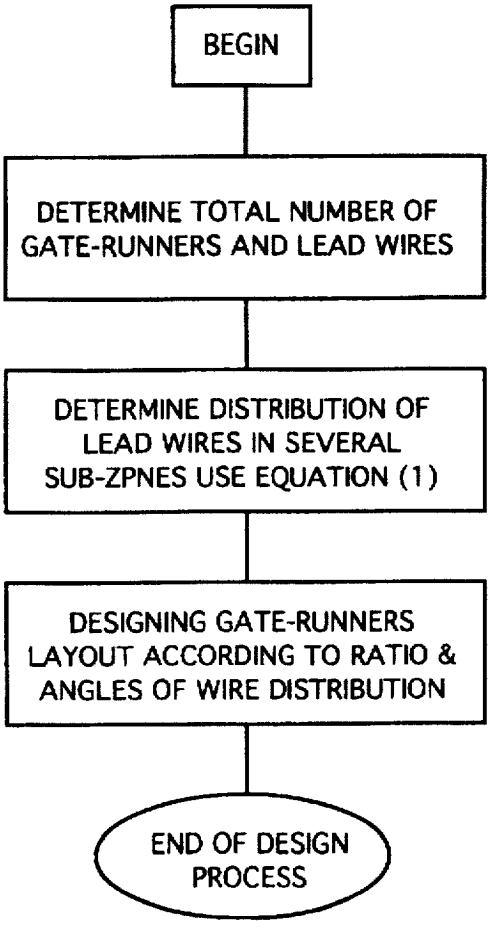

BEGIN
DETERMINE TOTAL NUMBER OF GATE-RUNNERS AND LEAD WIRES
DETERMINE DISTRIBUTION OF LEAD WIRES IN SEVERAL SUB-ZPNES USE EQUATION (1)
DESIGNING GATE-RUNNERS LAYOUT ACCORDING TO RATIO & ANGLES OF WIRE DISTRIBUTION
END OF DESIGN PROCESS

FIG. 5

DESIGN OF DEVICE LAYOUT FOR INTEGRATION WITH POWER MOSFET PACKAGING TO ACHIEVE BETTER LEAD WIRE CONNECTIONS AND LOWER ON RESISTANCE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the device layout and packaging process of power MOSFETs. More particularly, this invention relates to a novel and improved device layout and packaging process for fabricating a power MOSFET device to achieve lower drain to source resistance by lowering the spreading resistance.

2. Description of the Prior Art

Conventional device layout and packaging configuration for fabricating a power metal oxide silicon field effect transistor (MOSFET) power device are limited by the technical difficulty that the on-resistance is increased due to the contact point arrangements of lead wires to the source contact. Specifically, conventional device layout and the lead-wire connection configuration of power MOSFETs, by the of use of either gold wires or aluminum wires, result in higher spread resistance which leads to higher on-resistance.

The difficulty arises from the facts that the device layout of the power MOSFET is designed and manufactured before the transistor is packaged. However, in the process of packaging the transistor, additional lead wires are formed onto the transistor for making connection of the transistor with the pins on the package serving as means for providing external interface. In forming the lead wires onto the transistor contacts, the performance characteristics, e.g., the on-resistance, are impacted. Since the power MOSFET and the package are designed in two separate stages, the impacts on performance characteristics of the power MOSFET due to packaging processes are not taken into consideration in the design stage for the power MOSFET.

FIG. **1A** shows a typical power MOSFET package **10** which includes a MOSFET device **15**, i.e., the chip, connected to lead frames **20** by the use of lead wires **25**, e.g., gold wires with a diameter of approximately 2 mils. The MOSFET device **15** includes a plurality of gate-metal stripes, i.e., the gate runners **30**. The gate runners **30** divide the source contact surface into several equally divided areas, e.g., **35-1**, **35-2**, **35-3**, **35-4**, and **35-5**. The lead wires **25** are then formed to connect the lead frames **20** to the surface of source contact, e.g., **35-1** to **35-5**. For the convenience of fabrication and cost savings, the wires **25** are formed to disposed on the source contact surface near the lead frames **20** such that the wires are shorter and easier to maneuver in the wiring processes. However, since the wires **25** are not evenly distributed in the source contact surface, for a point, e.g., point **45**, which is located in an area far away from the lead frame **20**, there is a spread distance, Ls, between the wire-to-source contact point **40**. A drain to source current initiated from the source underneath point **45** has to travel a longer spread distance Ls to reach the lead-to-source contact point **40**. The longer the distance Ls, the greater the spread resistance Rs which is generally proportional to the length of the current path. The facts that the source contact surface **35-1** to **35-5** is equally divided by the gate runners **30** and that the lead-wires **25** are randomly formed on one end of the contact surface **35**, cause a higher spread resistance thus unduly increasing the on-resistance of the MOSFET device **15** under this device layout and packaging configuration.

FIG. **1B** shows another conventional packaging configuration for a power MOSFET device **50** which employs a

plurality of aluminum wires **60**, which are typically wires of 15 mils in diameter, for connecting to the lead frames **70**. Again, the gate runners **75** divide the source contact surface into equal areas **80-1** to **80-4**. Due to the facts that wedge bonding process has to applied to bond the aluminum wires **60** to the source contact surface **80-1** to **80-4** and that the angle of the wire from the wedge bonding pad should be less than 60 degrees, the gate runners **75** are arranged to have middle openings to allow the aluminum wires **60** to turn an angle for making connection to the lead frame **70**. However, in this configuration, again, the on resistance for the MOSFET device **50** is increased due to the fact that the contact points between the aluminum wires **60** and the source contact surface **80-1** to **80-4** are unevenly distributed. These contact points are long distance away from some source contact points which leads to high spread resistance and in turn causing the on-resistance to increase.

Therefore, there is still a need in the art of power device fabrication, particularly for power MOSFET design and fabrication, to provide a improved design for device layout for integration with the MOSFET packages such that these limitations and difficulties can be resolved.

SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide an improved design for device layout of the power MOSFET to overcome the aforementioned difficulties encountered in the prior art.

Specifically, it is an object of the present invention to provide an improved MOSFET device layout and packaging configuration wherein novel gate runner and source contact topology are arranged to evenly distribute the wire lead contacts thus lowering the spread resistance and the on-resistance.

Another object of the present invention is to provide an improved MOSFET device layout and packaging configuration where the source contact areas divided by the gate runners are flexibly arranged to be proportional to the number of the lead contacts formed in each divided area such that the lead wire contacts are more evenly distributed on the surface of the source contact.

Another object of the present invention is to provide an improved MOSFET device layout and packaging configuration wherein the layout of the gate runners and the source contact areas are flexibly arranged for integrating with the lead wire and lead frame configuration such that the lead wires for source contact connections can be optimally formed to reduce the spread resistance.

Another object of the present invention is to provide an improved MOSFET device layout and packaging configuration wherein the layout of the gate runners and the source contact areas are flexibly arranged which are more suitable for wedge bonding when the aluminum lead wires are employed to simplify the fabrication process and to lower the on resistance.

Briefly, in a preferred embodiment, the present invention includes a MOSFET power integrated circuit (IC) device disposed in a semiconductor chip including a source contact area which is provided for connecting to a lead-frame via a plurality of lead-wires. The power IC device includes a plurality of lead-wire contact points disposed on the source contact area for securely attaching the lead wires thereon wherein the lead-wire contact points are disposed substantially in a uniform distribution over the source contact area.

In an alternate preferred embodiment, this invention discloses a power integrated circuit (IC) device disposed in a

semiconductor chip including a source contact area provided with a plurality of lead-wire contact points thereon for connecting to a lead-frame via a plurality of lead-wires to be securely attached to the source contact area on each of the lead-wire contact points. The IC device includes a plurality of gate runners disposed on the source contact area thus dividing the source contact area into several sub-contact areas wherein the several sub-contact areas are arranged with different sizes for substantially distributing the lead-wire contact points uniformly over the source contact area.

In yet another preferred embodiment, this invention discloses an integrated circuit (IC) power device disposed in a semiconductor chip including a source contact area provided with a plurality of lead-wire contact points thereon for connecting to a lead-frame via a plurality of lead-wires to be securely attached to the source contact area on each of the lead-wire contact points. The power IC device includes a plurality of gate runners disposed on the source contact area thus dividing the source contact area into several sub-contact with slant angles for alignment with the lead-wires for connecting to the lead-frames.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment which is illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1A** and **1B** are top views showing conventional device layout and packaging configurations for power MOSFET employing gold wires and aluminum wires respectively;

FIGS. **2A** to **2D** are the cross sectional view and top view respectively of a novel device layout and packaging configuration for a power MOSFET of the present invention;

FIG. **3** is a top view showing a novel device layout with the gate runners slanted toward the lead frames thus dividing the source contact area into slanted sub-regions and more suitable to form wedge bond in the sub-region for the aluminum wires;

FIG. **4** is a cross sectional view of the aluminum wire with stitch contacts distributed over the source contact areas to evenly distribute the contact points thus reducing the spread resistance; and

FIGS. **5** is a flow chart showing the design process for design the device layout with different gate runner arrangements to achieve optimal packaging and device performance characteristics.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to FIGS. **2A** and **2B** for a cross sectional view and top view respectively of a power MOSFET device **100** with novel topology of the gate-runner arrangement. The MOSFET device **100**, i.e., the chip, is mounted on a die pad **110** surrounded by lead frames **120**. The lead frames **120** are then connected to different pins, e.g., pin **1** to pin **8** as shown, for external interface. The MOSFET device **100** includes a gate contact **130** which is connected to pin **4** with a lead wire **135**. The MOSFET device **100** further includes a plurality of gate runners **140** which divide the source contact **150** into several source contact areas, e.g., source contact areas **150-1**, **150-2**, **150-3**, and **150-4**. A plurality of lead wires **160** are then formed for connecting the source contact **150** to the lead frames **120**. According a principle of this invention, in order to reduce the spread resistance, the topology of the gate runner **140** specially arranged according to the location of the lead frames and the external pins, e.g., pin **1** to pin **4**, for dividing the source contact areas **150-1** to **150-4** to source contact areas of unequal sizes. Furthermore, the contact points **170**, where the lead wires **160** are connected to the source contact **150**, are spread out in each of the contact areas **150-1** to **150-4**. The division of the contact areas **150-1** to **150-4** and the spread of the contact points **170** between the lead wire **160** to source contact **150** are arranged to achieve reduced spread resistance. The number of gate runners **140** depends on the device characteristics. For large devices, more gate runners **140** are used to reduce the gate resistance and improve the switching speed. In addition to the number, i.e., N_{GR}, of gate runners **140**, the ratio of the contact areas for uniformly distributing the wires **160** in several contact area divided by the gate runners **140** also depends on the number, i.e., N_{LW}, of the lead wires **140**. In general, the number N_{LW} of lead wire wires **140** is determined by: a) the number of wires the device needs, i.e., N_{NEED} and b) the number of wires the lead frame can accommodate, i.e. N_{FRAME}.

$$N_{LW}=\text{Minimum}\{N_{NEED}, N_{FRAME}\} \quad (1)$$

A basic number of wires to be distributed in each of the contact areas N_{BASIC} is:

$$N_{BASIC}=\text{Integer of}\{N_{LW}/(N_{GR}+1)\} \quad (2)$$

and

$$N_{LW}=(N_{GR}+1)N_{BASIC}+N_{REMAINER} \quad (3)$$

Where $N_{REMAINER}$, i.e., the remainder of equal of distribution, has an integer value ranging between zero and $(N_{BASIC}-1)$. In order to more evenly distribute the lead wires **160** into $(N_{GR}+1)$ contact areas, a simple basic rule is established to divide the lead wires into $(N_{GR}+1)$ groups where:

$$N_{LW}=N(1)+N(2)+\ldots+N(K)+N(K+1)+\ldots+N(GR+1) \quad (4)$$

Where $N(1)=N(2)=N(3)=\ldots=N(K)=N_{BASIC}$, and $N(K+1)=N(K+2)\ldots=N(GR+1)=(N_{BASIC}+1)$ and $K=(N_{GR}+1)-N_{REMAINDER}$. The above basic rule can be easily understood with an example, for instance, the total number of lead wires, i.e., N_{LW}, is 19, the number of gate runners N_{GR} is 4, a basic equal distribution is N_{BASIC} is 3 and a remainder of equal distribution $N_{REMAINDER}$ is 4. The lead wires are distributed into five groups with a distribution ratio of {3:4:4:4:4}, i.e., a distribution according to Equation (4), where $K=(4+1)-4=1$ and $(N_{BASIC}+1)=4$. Based on this ratio, the contact areas **150** are then divided by the gate runners **140** to have substantially the same ratio.

In the preferred embodiment shown in FIGS. **2A** and **2B**, with three gate runners **140**, the source contact area **150** are divided, according to the above basic equal distribution rule, into four sub-contact areas having a proportion of approximately 4:4:4:3 between the contact areas **150-1** to **150-4**. The lead wire **160** are then arranged to spread out in each of the contact areas **150-1** to **150-4**. A simplified method is applied to spread the lead wire contact points **170** in each of the contact source areas **150-1** to **150-4** by dividing the width, i.e., W, and length, i.e., L, into equal segments of ΔX and ΔY, i.e., $\Delta X=W/N$ and $\Delta Y=L/N$, and then placing the contact points **170** on the point $(k\Delta X, k\Delta Y)$ where k=1 to N and N is the number of wire leads placed into that area, e.g., N=4 for source contact areas **150-1** to **150-3**, and N=3 for

source contact area **150-3**. By spreading the points of contact **170** in each of these areas, for a power MOSFET device **100** of size of W=98 mils and L=160 mils (which have die pad size of approximately 106 mils by 166 mils), the spread resistance is reduced from a range of 12 to 15 milli-ohms to approximately 7 to 10 milli-ohms. The improvement in spread resistance may depend on the device characteristics. For a 30-volts device, about ten to twenty percents (10%–20%) of the total on-resistance are caused by the spread resistance, while the percentage for a lower 12-volts device can be as high as thirty to fifty percents (30–50%) due to the spread resistance. Generally, by applying the design rules disclosed in this invention, greater improvements in performance are achieved for lower voltage device.

FIGS. 2C and 2D are top views of two alternate embodiments of a power MOSFET device similar to that shown in FIGS. 2A and 2B, except that the gate runners **140** are arranged differently. These types of gate runner arrangements are implemented for die size reduction and speed improvement.

Therefore, in a preferred embodiment, the present invention includes a MOSFET power integrated circuit (IC) device **100** disposed in a semiconductor chip **110** including a source contact area **150** which is provided for connecting to a lead-frame **120** via a plurality of lead-wires **160**. The power IC device includes a plurality of lead-wire contact points **170** disposed on the source contact area **150** for securely attaching the lead wires **160** thereon wherein the lead-wire contact points **170** are disposed substantially in a uniform distribution over the source contact area **150**.

In an alternate preferred embodiment, this invention discloses a power integrated circuit (IC) device **100** disposed in a semiconductor chip **110** including a source contact area **150** provided with a plurality of lead-wire contact points **170** thereon for connecting to a lead-frame **120** via a plurality of lead-wires **160** to be securely attached to the source contact area **150** on each of the lead-wire contact points **160**. The IC device includes a plurality of gate runners **140** disposed on the source contact area **150** thus dividing the source contact area into several sub-contact areas **150-1**, **150-2**, **150-3**, and **150-4** wherein the several sub-contact areas **150-1** to **150-4** are arranged with different sizes for substantially distributing the lead-wire contact points **170** uniformly over the source contact area **150**.

This invention also discloses a method to configure a source contact area **150** on a power MOSFET device **100** by dividing said source contact areas **150** with several gate runners **140** disposed thereon, the method including steps of: (a) determining a total number of lead wires **160** for connecting to a lead frame **120** from the source contact area **150** on the MOSFET power device **100**; and (b) configuring the gate runners **140** for dividing the source contact area **150** into several sub-contact areas **150-1** to **150-4** with a set of area proportional ratios, e.g., 4:4:4:3, for disposing several of the lead wires **160** in each of the sub-contact areas **150-1** to **150-4** according to the set of area proportional ratios, e.g., 4:4:4:3.

Please refer to FIG. **3** for a top view showing a novel device layout and packaging configuration for a power MOSFET **200** of the present invention. The power MOSFET device **200** includes a plurality of gate runners **210** which divide the source contact area into a plurality of sub-regions, e.g., sub-regions **220-1**, **220-2**, **220-3**, and **220-4**. In each sub-region, there is a aluminum wire **230** connecting the source contact area **220-2** to **220-4** to a lead frame **240** surrounding the MOSFET chip **205**. The device layout is modified to align with a angular slant toward the lead frame **240** such that it is easily integratable with lead frame **240**. Specifically, the aluminum wire **230** in this layout can be formed in each of these contact sub-regions **220-1** to **220-4** with a wedge bonding directed to the lead frame **240**. The aluminum wire **210** can therefore be formed by employing a wedge bonding **250** without an angular turn as that required in the prior art. More reliable packaging is achieved because the straight wire arrangement.

Thus, this invention discloses an integrated circuit (IC) power device **200** disposed in a semiconductor chip **205** including a source contact area **220** provided with a plurality of lead-wire contact points **250** thereon for connecting to a lead-frame **240** via a plurality of lead-wires **230** to be securely attached to the source contact area **220** on each of the lead-wire contact points **250**. The power IC device **200** includes a plurality of gate runners **210** disposed on the source contact area **220** thus dividing the source contact area into several sub-contact areas **220-1**, **220-2**, **220-3**, and **220-4** with slant angles for alignment with the lead-wires **230** for connecting to the lead-frames **240**.

Please refer to FIG. **4** for additional improvement to reduce the MOSFET spread resistance of the aluminum wire connection. Instead of a single aluminum wire contact point to the source contact surface **220-4** to **220-4**, the aluminum wire are formed to have "stitch contacts" **250** with the source contact areas **220-2** to **220-4**. The purpose of the stitch contacts is to generate more points of wire-source contact such that the contact points **250** are more evenly distributed in each of the source contact sub-regions **220-1** to **220-4**. The spread resistance is therefore reduced with more numerous and more evenly distributed contacts in each sub-regions.

The basic design rule is to evenly distribute the wires **230** and the contact points **250** over the contact areas **220-1** to **220-4** which are divided by the gate runners **210**. Typically, for a device package which employs aluminum wires **230**, only one to two wires are distributed in each slanted contact area, e.g., **220-2** to **220-4**. The distance between stitch contact points **250** can be flexibly arranged depending on the machine capability and the production costs involved in making these stitch contacts. The stitch contact points can be formed for each aluminum wire **230** to have distance of several mils or with even smaller distance. A measurable improvements of five to almost twenty percents (5–20%) of the spread resistance, and thus correspondingly the on-resistance, are achievable because of the more uniform distribution of the contact points over the source contact areas.

Referring to FIG. **5** for a flow chart for design the layout configuration of a source contact area **150**. To start the design process (step **300**), the total number N_{GR} of gate runners **140** and the lead wires **160**, i.e., N_{LW}, for connecting to a lead frame **120** are first determined (step **310**). The ratios of lead wires **160** to be distributed in $N_{GR}+1$ sub-contact regions, e.g., **150-1** to **150-4**, are then computed according to Equations (1) to (4), (step **320**). The layout of the gate runners **140** are then designed (step **330**) according to the ratios determined in step **320**. Similarly, for designing a layout of the source contact area when the aluminum wires are employed, the slant angles of the lead wires are first determined based on the relative location of the chip and lead frame. Then the layout of the gate runners are determined to comply with the slant angles required for the wedge bonding pads used for attaching the aluminum lead wires such that the lead wire twist may be minimized.

Therefore, the present invention provides an improved design for device layout and packaging configuration for

manufacturing the power MOSFET to overcome the difficulties encountered in the prior art. Specifically, an improved MOSFET device layout and packaging configuration are provided wherein novel gate runner and source contact topology are arranged to evenly distribute the lead wire contacts on the source contact surface thus lowering the spread resistance and the on-resistance. The source contact areas divided by the gate runners are now flexibly arranged to be proportional to the number of the lead contacts formed in each divided area such that the lead wire contacts are more evenly distributed on the surface of the source contact. The gate runners and the source contact areas are flexibly arranged for integrating with the lead wire and lead frame configuration such that the lead wires for source contact connections can be optimally formed with the packaging configuration to reduce the spread resistance. In a MOSFET device package where aluminum wires are employed, the gate runners and the source contact areas are flexibly arranged with an angular slant toward the lead frame which are more suitable for wedge bonding. Furthermore, stitch contacts are formed to more evenly distributed the contact points on the source contact surface such that the spread resistance can be reduced.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alternations and modifications will no doubt become apparent to those skilled in the art after reading the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alternations and modifications as fall within the true spirit and scope of the invention.

We claim:

1. A power integrated circuit (IC) device disposed in a semiconductor chip including a source contact area provided with a plurality of lead-wire contact points thereon for connecting to a lead-frame via a plurality of lead-wires to be securely attached to said source contact area on each of said lead-wire contact points, said IC device comprising:

a plurality of gate runners disposed on said source contact area thus dividing said source contact area into several sub-contact areas wherein said several sub-contact areas are arranged with different sizes for substantially distributing said lead-wire contact points uniformly over said source contact area.

2. A power integrated circuit (IC) device disposed in a semiconductor chip including a source contact area provided with a plurality of lead-wire contact points thereon for connecting to a lead-frame via a plurality of lead-wires to be securely attached to said source contact area on each of said lead-wire contact points, said IC device comprising:

a plurality of gate runners disposed on said source contact area thus dividing said source contact area into several sub-contact areas with slant angles for alignment with said lead-wires for connecting to said lead-frames.

3. The integrated circuit (IC) power device of claim 2 wherein:

each of said lead wires for connecting to said lead frames includes several stitch contact points attaching to a top surface of said source contact area thus increasing said lead wire contact points disposed on said source contact area.

4. The integrated circuit (IC) power device of claim 2 wherein:

each of said lead wires is an aluminum wire and each of said lead wire contact points includes a wedge bonding pad for securely attaching said aluminum wires to said top surface of said source contact area.

5. A MOSFET power device disposed in a semiconductor chip including a source contact area provided with a plurality of lead-wire contact points thereon for connecting to a lead-frame via a plurality of lead-wires to be securely attached to said source contact area on each of said lead-wire contact points, said IC device comprising:

a plurality of gate runners disposed on said source contact area thus dividing said source contact area into several sub-contact areas wherein said several sub-contact areas are arranged with different sizes for substantially distributing said lead-wire contact points uniformly over said source contact area.

6. The MOSFET power device of claim 5 wherein:

said plurality of gate runners disposed on said source contact area dividing said source contact area into several sub-contact areas of substantially equal size for disposing an evenly-distributed equal number of said lead wire contact points therein with a remainder number of sub-contact areas having smaller areas for disposing a less lead wire contact points therein wherein said less wire contact points being one less than said evenly distributed equal number of said wire contact points.

7. A method to configure a source contact area on a power MOSFET device by dividing said source contact areas with several gate runners disposed thereon, said method including steps of:

(a) determining a total number of lead wires for connecting to a lead frame from said source contact area on said MOSFET power device; and

(b) configuring said gate runners for dividing said source contact area into several sub-contact areas with a set of area proportional ratios for disposing several of said lead wires in each of said sub-contact areas according to said set of area proportional ratios.

8. A method to configure a source contact area on a power MOSFET device by dividing said source contact areas with several gate runners disposed thereon, said method including steps of:

(a) determining a total number of lead wires and angles of bonding pads for connecting to a lead frame from said source contact area on said MOSFET power device; and

(b) configuring said gate runners according said total number of lead wires and said angles of bonding pads for designing a layout of said gate runners in said source contact area.

* * * * *

EXHIBIT 4

US005907776A

United States Patent [19]

Hshieh et al.

[11] Patent Number: 5,907,776

[45] Date of Patent: May 25, 1999

[54] **METHOD OF FORMING A SEMICONDUCTOR STRUCTURE HAVING REDUCED THRESHOLD VOLTAGE AND HIGH PUNCH-THROUGH TOLERANCE**

[75] Inventors: **Fwu-Iuan Hshieh**, Saratoga; **Koon Chong So**, San Jose, both of Calif.

[73] Assignee: **MagePower Semiconductor Corp.**, San Jose, Calif.

[21] Appl. No.: **08/891,546**

[22] Filed: **Jul. 11, 1997**

[51] **Int. Cl.**[6] **H01L 21/336**

[52] **U.S. Cl.** **438/270**; 438/273; 438/589

[58] **Field of Search** 438/268, 269, 438/270, 271, 272, 589, 273, 274; 148/DIG. 126

[56] **References Cited**

U.S. PATENT DOCUMENTS

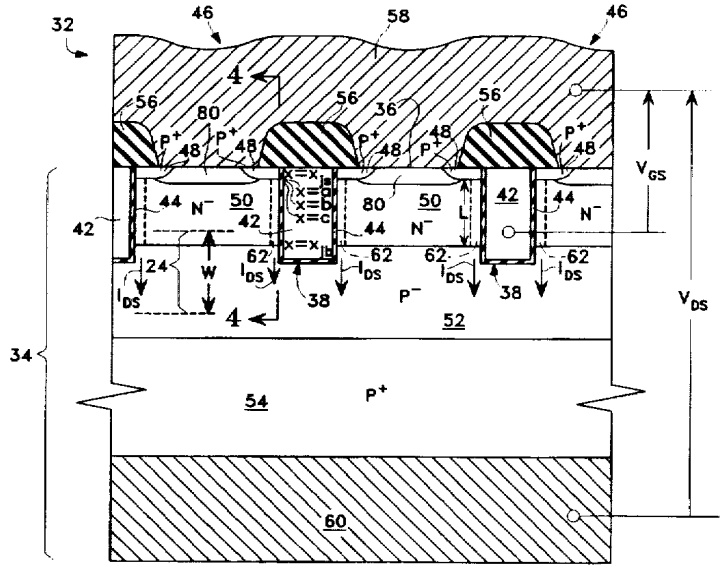
4,742,015	5/1988	Ohagen	438/237
5,135,880	8/1992	Fisher et al.	438/268
5,248,627	9/1993	Williams	438/268
5,527,720	6/1996	Goodyear et al.	438/270
5,567,634	10/1996	Hébert et al.	438/270
5,648,288	7/1997	Williams et al.	438/217

Primary Examiner—Michael Trinh
Attorney, Agent, or Firm—Kam T. Tam

[57] **ABSTRACT**

A power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) device formed on a semiconductor substrate having a body region of a first conductivity type diffused in a semiconductor substrate with an epitaxial layer of a second conductivity type. There is also a source region of a second conductivity type formed in the body region. A portion of the body region adjacent to the source region is compensated by ion implanting a material of the second conductivity type in the portion of the body region such that the impurity concentration of the body region at the portion is reduced. As a consequence, with reduced impurity charge in the body region adjacent to the source, the threshold voltage of the MOSFET device is lowered but at no comprise in punch-through tolerance because the reduction in charge is remote from the origin of the depletion layer which is located at the boundary between the body region and the epitaxial layer.

29 Claims, 6 Drawing Sheets



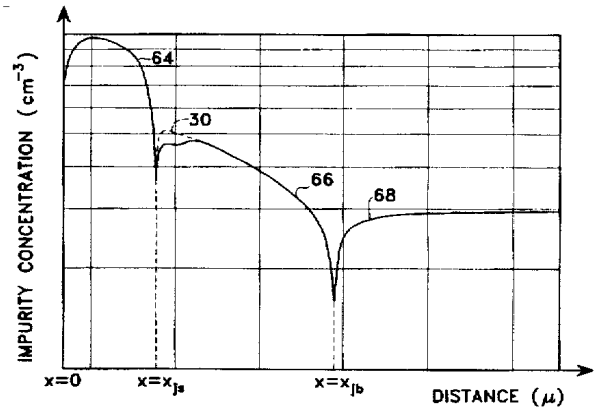


Fig. 1
(PRIOR ART)

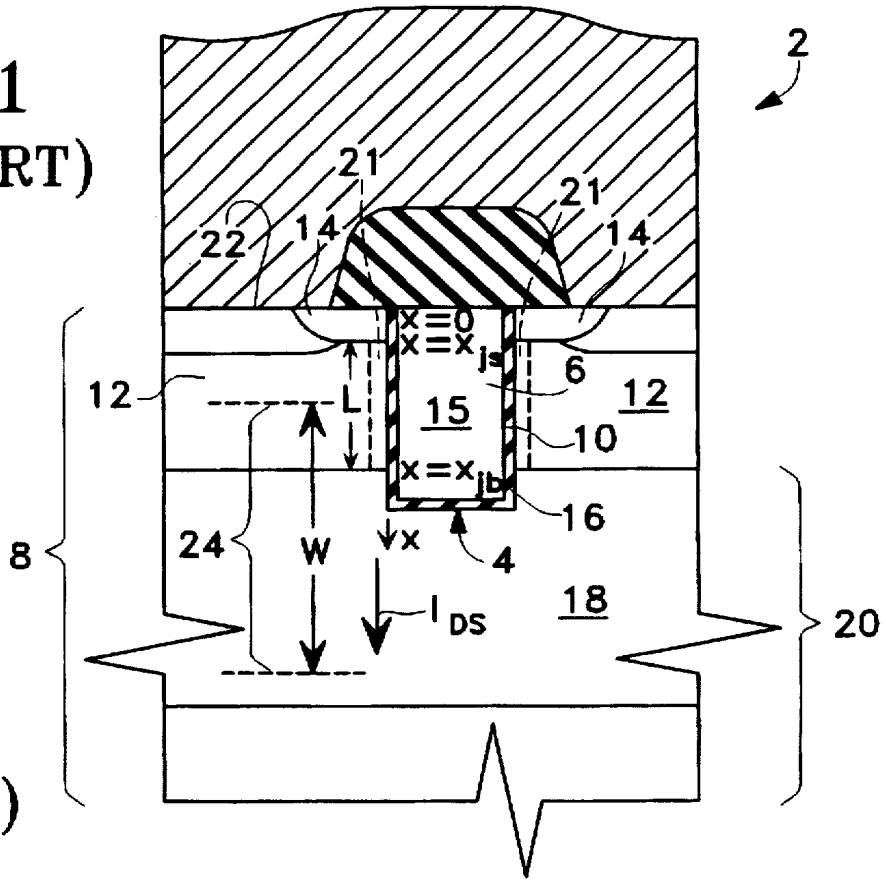
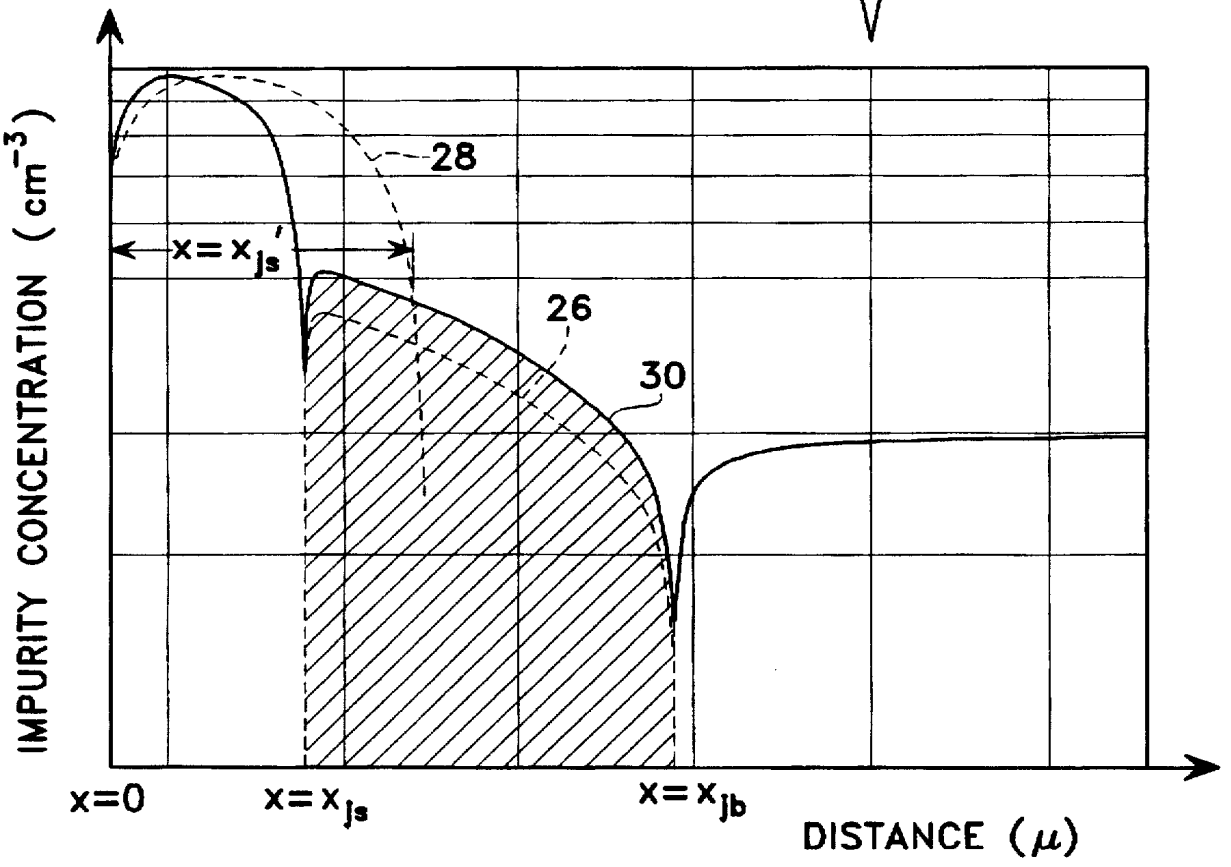


Fig. 2
(PRIOR ART)



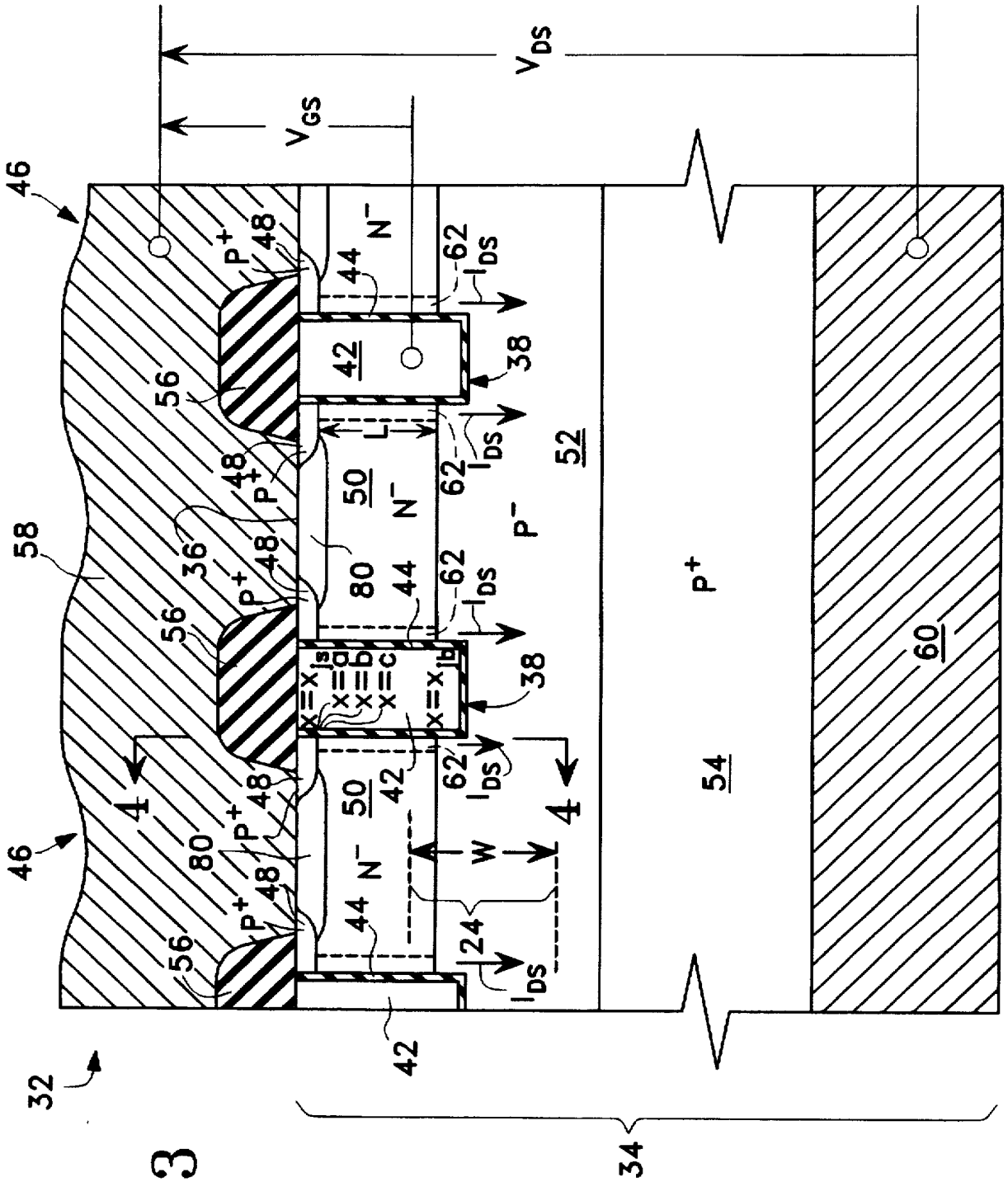

V_{DS}
V_{GS}
46
P^+
48
N^-
44
62
I_{DS}
42
38
56
L
50
52
P^-
P^+
58
36
80
x=a
x=b
x=c
60
54
4
W
24
32
34

Fig. 3

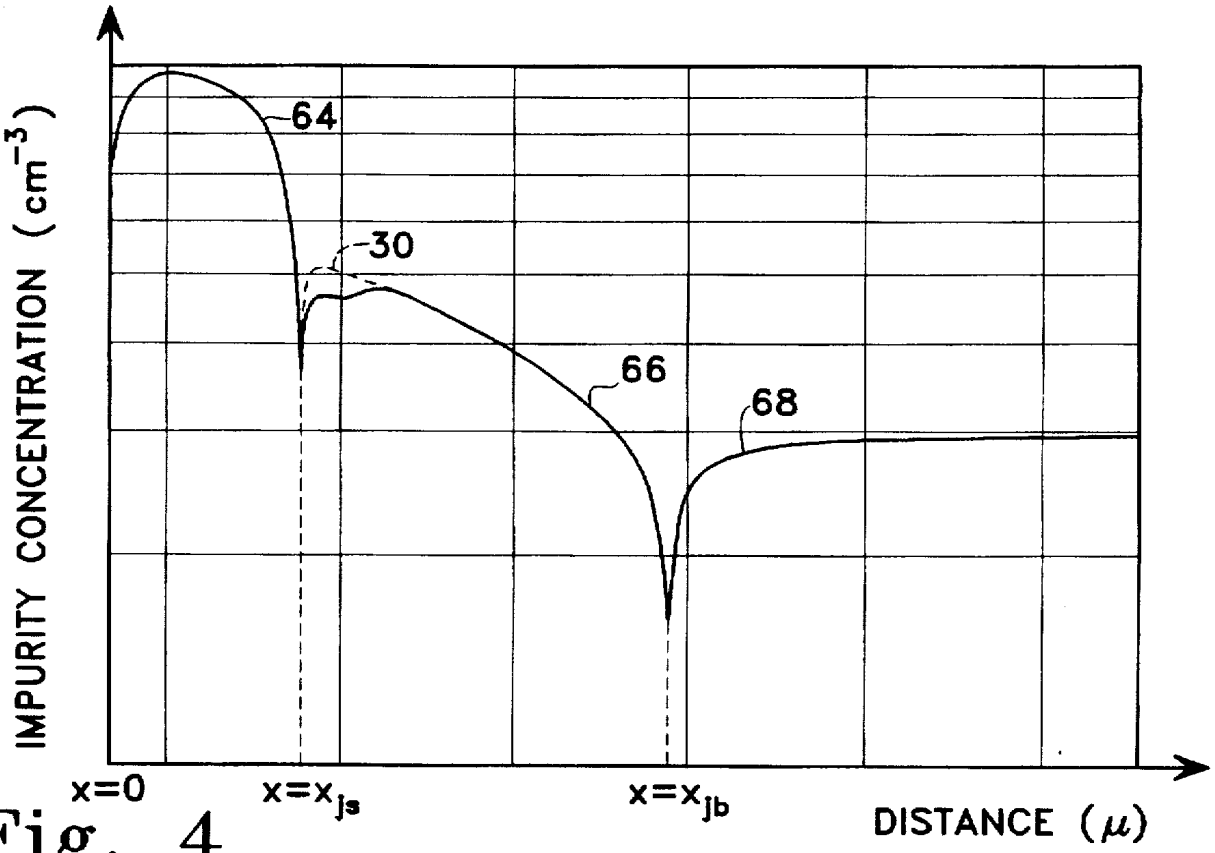
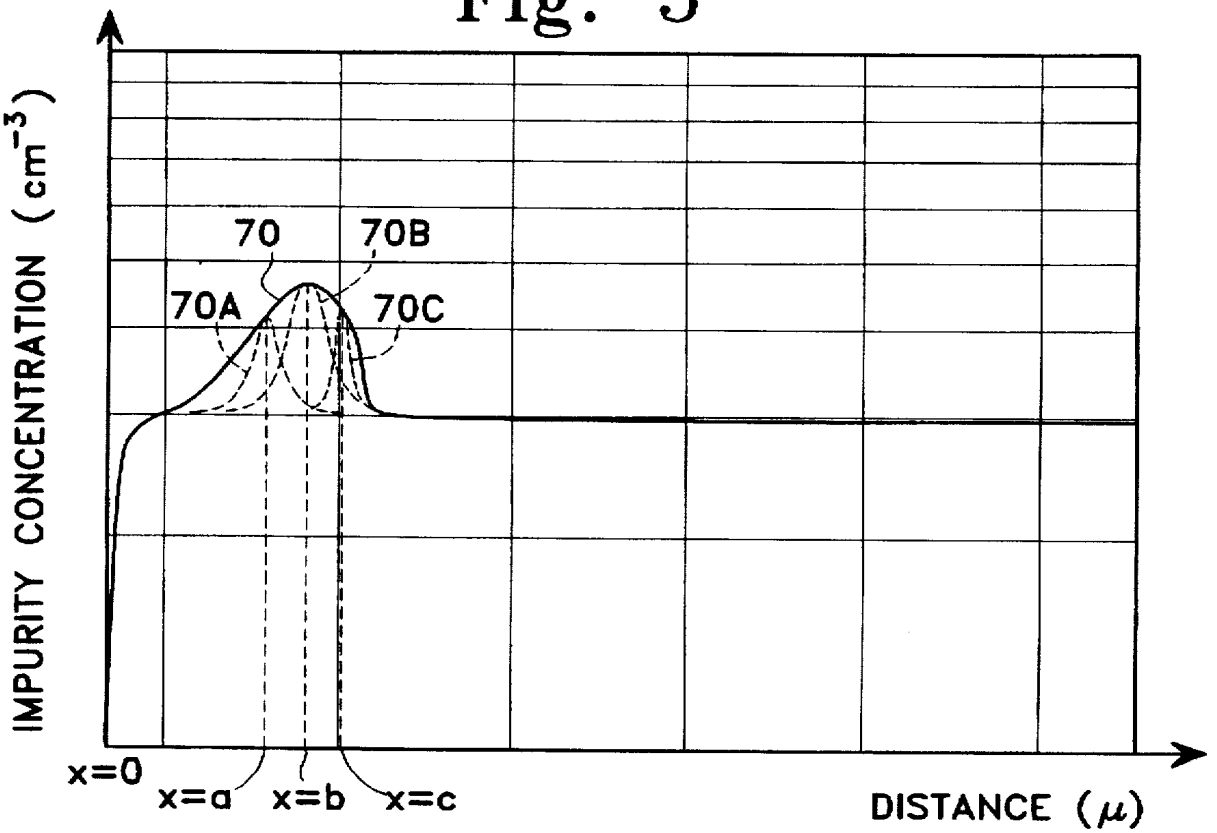

IMPURITY CONCENTRATION (cm^{-3})
64
30
66
68
x=0
$x=x_{js}$
$x=x_{jb}$
DISTANCE (μ)

Fig. 4

Fig. 5


IMPURITY CONCENTRATION (cm^{-3})
70
70B
70A
70C
x=0
x=a
x=b
x=c
DISTANCE (μ)

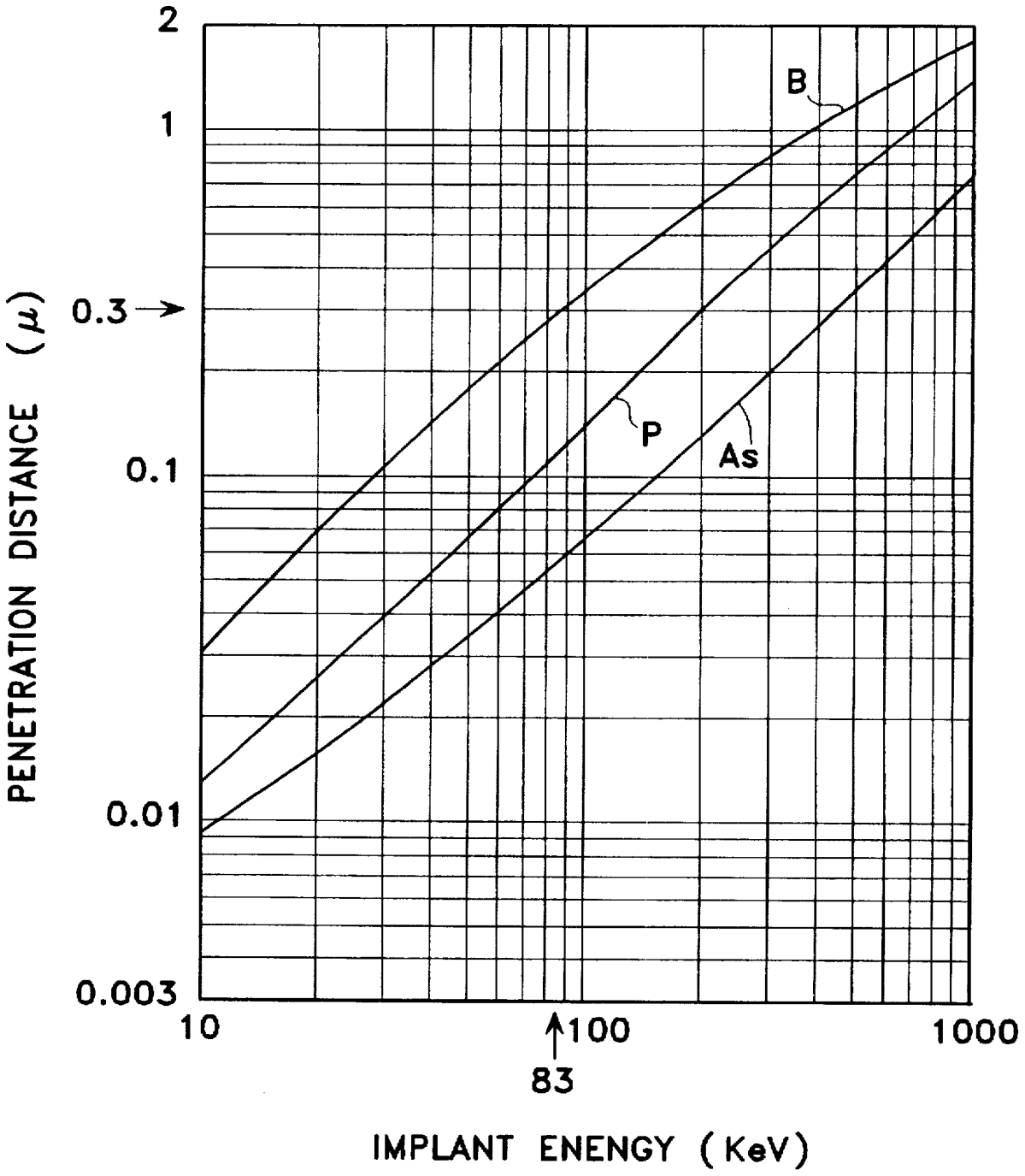

2
1
0.3
0.1
0.01
0.003
PENETRATION DISTANCE (μ)
B
P
As
10
100
1000
83
IMPLANT ENENGY (KeV)

Fig. 6

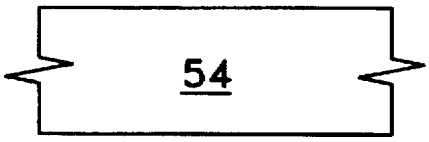


Fig. 7A

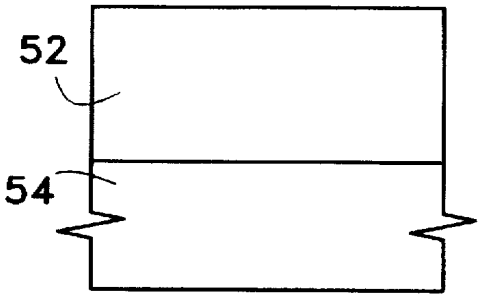


Fig. 7B

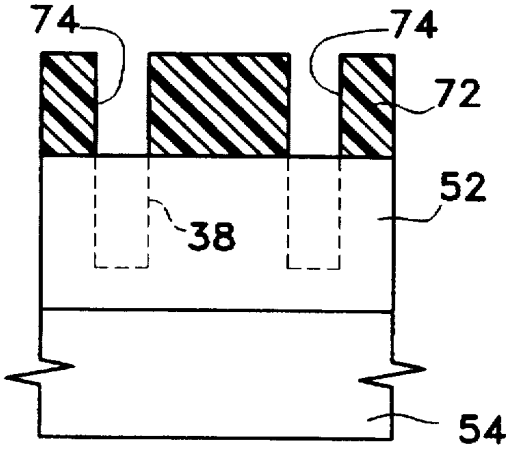


Fig. 7C

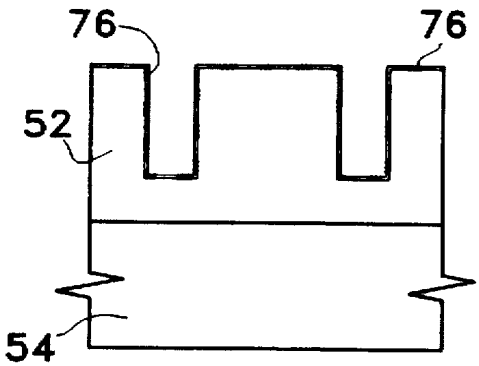


Fig. 7D

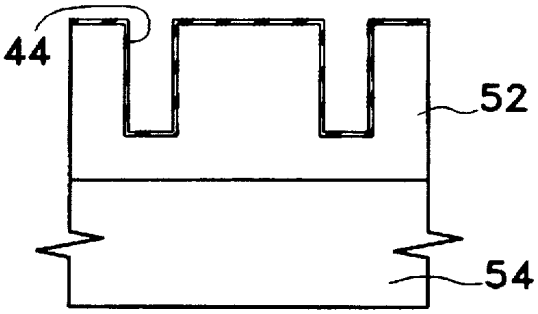


Fig. 7E

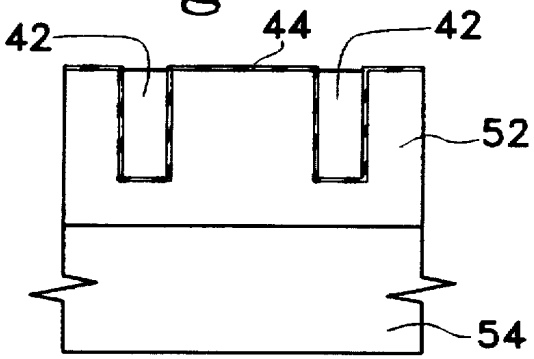


Fig. 7F

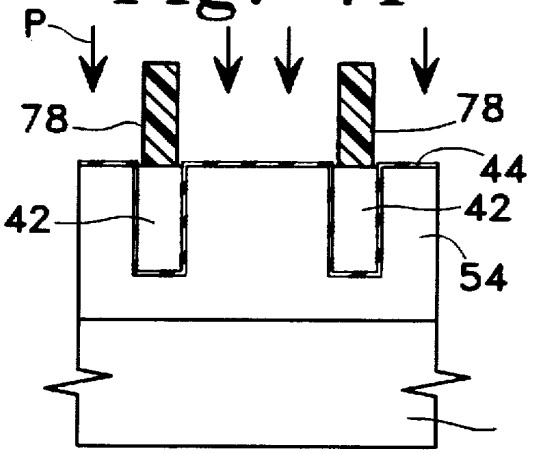


Fig. 7G

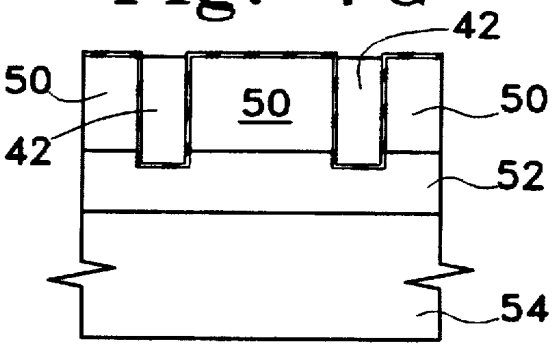


Fig. 7H

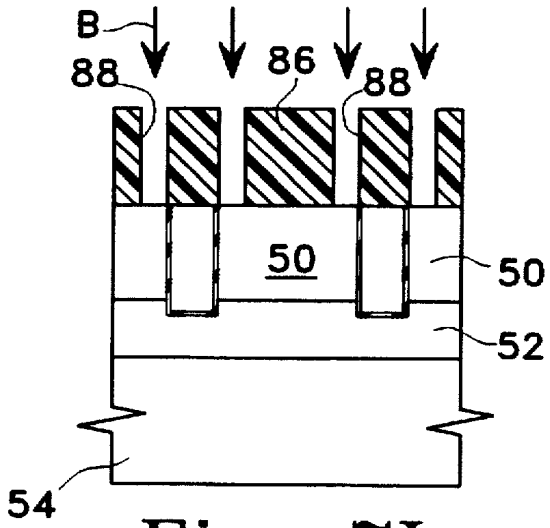


Fig. 7I

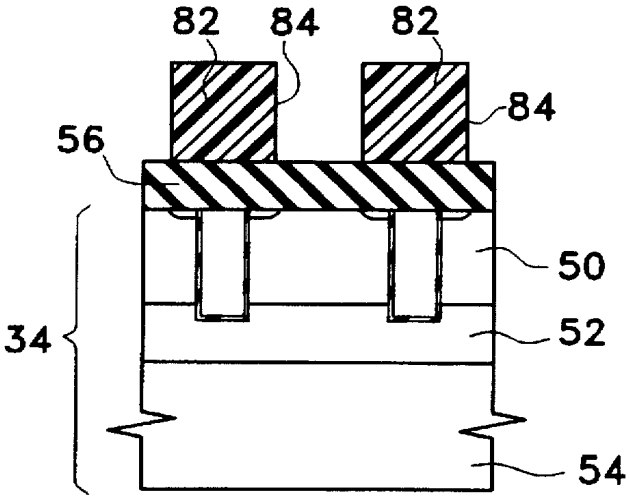


Fig. 7L

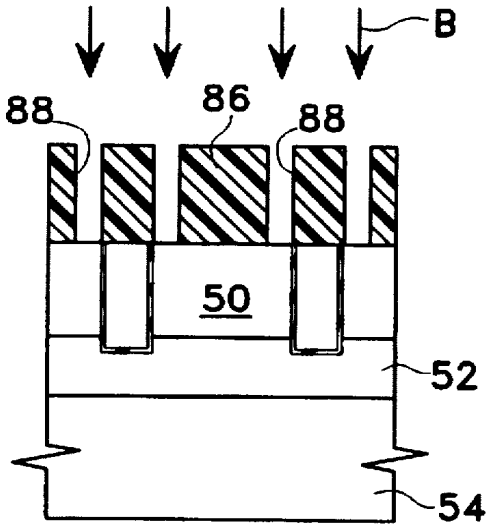


Fig. 7J

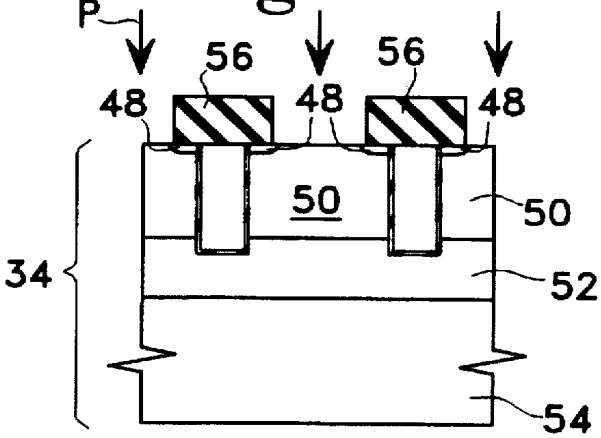


Fig. 7M

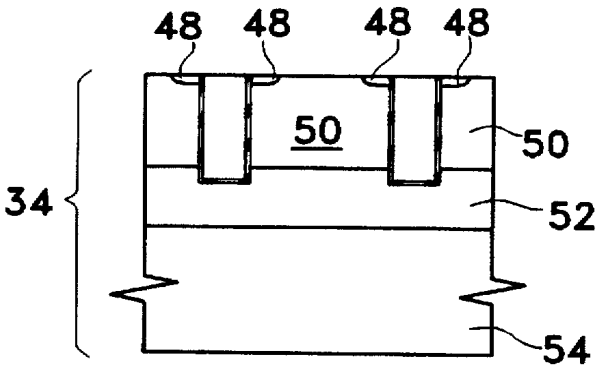


Fig. 7K

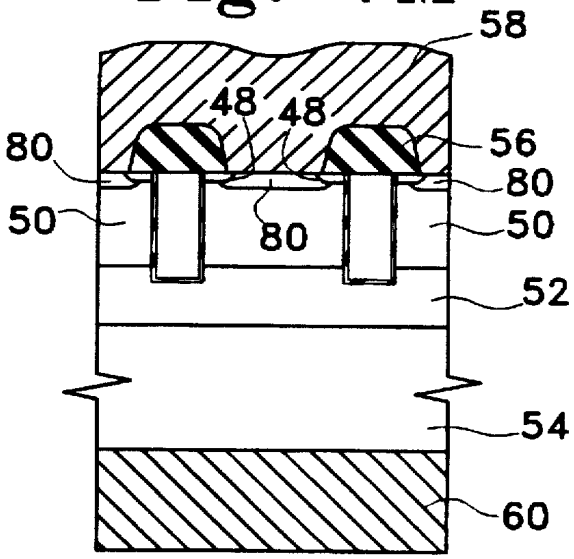


Fig. 7N

METHOD OF FORMING A SEMICONDUCTOR STRUCTURE HAVING REDUCED THRESHOLD VOLTAGE AND HIGH PUNCH-THROUGH TOLERANCE

BACKGROUND OF THE INVENTION

1 . Field of the Invention

The present invention relates generally to microelectronic circuits, and more particularly, to MOSFET (Metal Oxide Semiconductor Field Effect Transistor) power devices having reduced threshold voltage and high punch-through tolerance formed by the process of impurity concentration compensation.

2. Description of the Related Art

Power semiconductor devices have long been used as replacement for mechanical relays in various applications. Modern day instruments, now built at a miniaturized scale with lower power consumption, require power devices to operate under certain stringent requirements. For instance, in a hand-held cellular telephone or a laptop computer, it is common practice to reduce the main power supply level in order to preserve battery life. Accordingly, power devices suitable to be used in these instruments must be capable of operating under reduced power levels and with low turn-on resistance.

Metal oxide semiconductor field effect transistor (MOSFET) devices using trench gates provide low turn-on resistance and are often used for low power applications. In a trench MOSFET device, the channels are arranged in a vertical manner, instead of horizontally as in most planar configurations. The consequential benefit is the realization of a higher degree of integration on a semiconductor substrate. Furthermore, since the channel directions are vertical, the lateral current paths are basically eliminated. That is, each MOSFET cell assumes its own current path and there are no more shared current paths among cells. Stated differently, the vertical arrangement of the cell channels eliminates a dominant component of the turn-on resistance R_{ON}, called the junction resistance R_j, in each MOSFET cell inherently built in a planar configuration. The junction resistance R_j originates from the shared current paths among cells in a planar MOSFET device. The shared current paths essentially act as current bottle necks impeding the flow of channel current I_{DS} and are key contributors to the turn-on resistance R_{ON}. Elimination of the junction resistance R_j results in reduction in the turn on channel resistance R_{ON} and consequently curtails ohmic loss during the power-on state of the MOSFET. Lower ohmic loss provides lower power consumption and further alleviates heat dissipation.

FIG. **1** shows a cross-sectional view of a conventional trenched gate MOSFET device having a cell signified by the reference numeral **2**. The MOSFET cell **2** includes a trench **4** filled with conductive material **6** separated from the silicon substrate **8** with a thin layer of insulating material **10**. There are also other diffusion layers of different impurity types and concentrations deposited in the semiconductor substrate **8**. For examples, a source layer **14** is deposited in the body layer **12**, which in turn is diffused in an expitaxial layer **18**. As arranged, the conductive and insulating materials **6** and **10** in the trench **4** form the gate and gate oxide layer **16**, respectively, of the MOSFET. In addition, the depth L measured from the source **14** to the epitaxial layer **18** constitutes the channel length L of the MOSFET cell **2**. The epitaxial layer **18** is a part of the drain **20** of the MOSFET cell **2**.

When a potential difference is applied across the source **14** and the gate **15**, charges are capacitively induced in the body region adjacent to the gate oxide layer **16**. The induced charges in essence is an inversion layer and is called the channel **21** of the MOSFET cell **2**. When another potential difference is applied across the source **14** and the drain **20**, a drain-to-source current I_{DS} starts to flow from the source **14** to the drain **20** and the MOSFET **2** is said to be at the power-on state.

The conventional trenched MOSFET devices described above have an inherent high threshold voltage V_{th}, which is normally barely below the main power supply level required in a low power application. For example, in a low power instrument, the power supply V_{cc} is commonly set at 3 Volts, while the threshold voltage V_{th} of the MOSFET **2** sits at approximately 2.5 Volts. A turn-on voltage of 3 Volts applied to the gate **15** can hardly turn on the MOSFET device **2**. If the power supply is from a battery source, which drops in power supply V_{cc} level as time progresses, the MOSFET device **2** may never be turned on thereafter. Clearly, the conventional MOSFET **2** is not suitable to be used in applications with reduced V_{cc} levels. Thus, for the power device to function properly under reduced power supply conditions, the threshold level V_{th} of the MOSFET **2** has to be correspondingly reduced. Heretofore, various approaches have been attempted to reduce the threshold level of the MOSFET **2** but have not been proved successful.

Referring to FIG. **1**, the threshold voltage V_{th} is defined as the minimal potential difference between the gate **15** and the source **14** required to barely induce the channel **21** in the body layer **12**. The threshold voltage V_{th} is dependent upon a variety of factors including, inter alia, the thickness of the gate oxide **16**, and the impurity concentration of the body region **12**. The gate oxide thickness and the impurity concentration of the body region are more accessible parameters for adjustment, in contrast with other parameters such as the work functions or the Fermi levels of the basic materials of the MOSFET **2**, which parameters require higher degree of difficulty to manipulate. A precise mathematical expression for the threshold voltage V_{th} can be found in a publication by Wolf et al., "Silicon Processing for the VLSI Era", Lattice Press, IEEE Transactions on Electron Devices, Vol. 2, page 301.

Very often, the thickness of the gate oxide **16** is reduced to lower the threshold voltage V_{th}. However, the drawback with this approach is that making the gate oxide thickness thinner seriously undercut the final production yield and furthermore the reliability of the MOSFET. As is shown in FIG. **1**, the thinner the gate oxide layer **16**, the higher the probability of the conductive material **6** short-circuiting the other layers in the semiconductor substrate **8** through oxide defect in the gate oxide layer **16**.

The second approach to reduce the threshold voltage V_{th} is to lower the impurity concentration of the body layer **12**. However, results of this approach is also fraught with various problems.

FIG. **2** shows the diffusion profile of the MOSFET cell **2**. The abscissa axis of FIG. **2** represents the distance measured from the planar surface **22** toward the substrate **8** (FIG. **1**). The ordinate axis of FIG. **2** corresponds to the impurity concentration of the various layers in absolute value. For example, the source layer **14** is located at a distance of $x=x_{js}$ from the planar surface **22**. Similarly, the body layer **12** is positioned at a distance from $x=x_{js}$ to $x=_{jb}$.

During normal operation, the drain **20** and the body layer **12** are reversely biased. Consequently, a depletion layer is formed characterized by a depletion region **24** with a depletion width W as shown in FIG. **1**, in which the depletion

layer **24** is partly shown in hidden lines. As is well known in the art, the lighter the impurity concentration of a layer, the wider is the depletion width W extending into that layer. Referring back to FIG. **1**, if the body layer **12** is too lightly doped, the depletion layer **24** may encroach into the source layer **14** resulting in an undesirable effect called "punch-through". During punch-through, breakdown ensures in which drain-to-source current I_{DS} flows directly from the source **14** to the drain **20** without passing through the channel **21**. Specifically, as shown in FIG. **2**, the hatched area underneath the impurity curve from $x=x_{js}$ to $x=x_{jb}$ corresponds to the total charge stored in the body layer **12**. The threshold voltage V_{th} of the MOSFET cell **2** can be lowered by reducing the impurity concentration of the body region **12**, as is graphically shown by the lowered curve **26** shown in hidden line in FIG. **2**. It should be noted that the ordinate axis of FIG. **2** is in logarithm scale. A slight shift in the curve **26** corresponds to a substantial change in total charge. The lowering of the impurity concentration in the body layer **12** entails the widening of the depletion layer **24** and increases the possibility of the MOSFET **2** running into punch-through as described above.

There have also been attempts to diffuse the source region **14** to a deeper depth, as shown in FIG. **2** by another hidden line curve **28** intersecting with the original body diffusion curve **30** to form a new source junction at $x=x_{js}$. The purpose is to reduce the total charge stored in the body layer **12**. However, the encroachment problem of the depletion region **24** remains more or less the same because this time, the depletion layer **24** needs only to travel a shorter distance to reach punch-through.

Portable instruments and hand-held electronic products operated by batteries are now in high demand. These instruments and products are all operated by batteries with limited battery lives, at least until the next battery recharges. To preserve battery power and to ensure reliability, there has been a long-felt and increasing need to provide power devices capable of operating under reduced power levels and with low turn-on resistances, yet with robustness in punch-through tolerance.

SUMMARY OF THE INVENTION

It is accordingly the object of the invention to provide a power semiconductor device with low threshold voltage capable of operating at low power supply levels and low turn-on resistance, yet without any compromise in punch-through tolerance. The objective of providing such features in the power semiconductor device at low manufacturing cost is also sought.

The power MOSFET device of the invention is formed on a semiconductor substrate having a body region of a first conductivity type diffused in a semiconductor substrate with an epitaxial layer of a second conductivity type. There is also a source region of a second conductivity type formed in the body region. A predetermined portion of the body region adjacent to the source region is compensated in impurity concentration by ion implanting a material of the second conductivity type into the body region. As a consequence, with reduced impurity charge in the body region at the predetermined position, the threshold voltage of the MOSFET device is reduced. However, the punch-through tolerance of the MOSFET device is not affected because the reduction in charge is remote from the origin of the depletion layer which is located at the boundary between the body region and the epitaxial layer. The compensation process requires no special tooling and the increase in manufacturing costs is insignificant.

As will be explained later in this specification, a MOSFET device formed in accordance with the invention allows additional leeway to shorten the channel length, enabling the MOSFET device to be built with further lower power-on resistance. It also needs to be mentioned that with lower threshold voltage, it takes a shorter rise time to reach the lower threshold voltage level to turn on the device, thereby ensuring faster switching rate for the MOSFET cell.

These and other features and advantages of the invention will be apparent to those skilled in the art from the following detailed description, taken together with the accompanying drawings, in which like reference numerals refer to like parts.

DESCRIPTION OF THE DRAWINGS

FIG. **1**, as described above, is a cross-sectional view of a conventional MOSFET device showing the various diffusion layers;

FIG. **2**, as described above, is a diffusion profile of the MOSFET device of FIG. **1** illustrating the impurity concentration of the various layers;

FIG. **3** is a cross-sectional view of the preferred embodiment of the invention;

FIG. **4** is a diffusion profile of the MOSFET device of FIG. **3** illustrating the impurity concentration of the various layers;

FIG. **5** is a diffusion profile highlighting only the impurity concentration of the compensation dopant impinging upon the body layer;

FIG. **6** is a graphical representation illustrating the relationship between the penetration distance and the required implant energy; and

FIGS. **7A–7N** are sequential views illustrating the process of making the MOSFET device of the invention.

DETAILED DESCRIPTION OF THE INVENTION

Reference is now made to FIG. **3** which shows the cross-sectional view of the preferred embodiment of the invention. The semiconductor structure of the invention is generally signified by the reference numeral **32** which includes a substrate **34** having a planar surface **36**. Formed in the substrate **34** is a plurality of trenches **38** filled with conductive material **42** which is electrically separated from the substrate **34** by thin insulating layers **44**. In the preferred embodiment, the materials for the substrate **34**, conductive material **42** and the insulating layers **44** are respectively crystalline silicon (Si), polycrystalline silicon (Si), and silicon dioxide (SiO_2). Each cell **46** is a P-channel MOSFET which comprises a source layer **48** made of P-type material, a body layer **50** formed of N-type material, an epitaxial layer **52** made of a lightly doped P-type material, and a drain layer **54** based on a heavily doped P-type material. Atop the trenches **38** are passivation layers **56** insulating the conductive material **42** from a source contact metal layer **58**. The source contact metal layer **58** is disposed in contact with the substrate **34** via contact regions **80**. There is also a drain metal contact layer **60** attached to the drain **54** of the MOSFET **32**. The conductive material **42** in the each trenched gate **38** is electrically connected but is not shown in FIG. **3**.

When a potential difference V_{GS} exceeding the threshold voltage V_{th} is applied across the source layer **48** and the trenched gates **42** through the respective metal contact layer **58** and the gate contact (not shown), an N-type inversion

layer **62** is capacitively induced in the P-type body layer **50**. The inversion layer **62** is called the channel of the MOSFET cell **46**. The highly conductive channel **62** allows a channel current I_{DS} to flow from the source **48** to the drain **54** when another potential difference V_{DS} is applied across the source **48** and the drain **54** through the respective metal contact layers **58** and **60**.

It should be noted that in contrast with the prior art structure **2** as described above, and shown in FIG. **1** the channel length L can be built at a shorter dimension because there is no comprise in impurity concentration in the bulk of the body region **50**, as is herein explained.

Shown in FIG. **4** is the diffusion profile taken along the cross-sectional line **4—4** of FIG. **3**. The ordinate axis of FIG. **4** corresponds to the impurity concentration of the various layers in absolute value of the semiconductor structure **32**. For example, the impurity concentrations of the source region **48**, the body region **50** and the expitaxial region **52** are represented by the curves **64**, **66** and **68**, respectively. The source layer **48** is located at a distance of $x=x_{js}$ from the planar surface **36** (x=0). Similarly, the body layer **50** is positioned at a distance from $x=x_{js}$ to $x=x_{jb}$. It should be noted that in FIG. **4**, the excess impurity concentration for the body diffusion curve **66** adjacent to the source boundary $x=x_{js}$ is truncated. In contrast, the conventional body diffusion curve represented by the curve **30** shown in hidden lines in which the excess charge is clearly eminent. The leveling of the impurity profile for the body diffusion curve **66** adjacent to the source boundary $x=x_{js}$ serves important functions. First, the threshold voltage V_{th} is substantially reduced because of the reduced impurity concentration near the source boundary $x=x_{js}$ in the body region **50**. It should be emphasized again that even though the charge reduction shown in FIG. **4** appears to be a small proportional reduction in comparison to the total charge stored in the body region **50**, nevertheless, FIG. **4** is illustrated in a logarithm scale and the reduction in impurity charge is in fact a sizable amount. Secondly, the reduction in charge is remote from the body boundary $x=x_{jb}$ where the depletion region **24** originates and extends. Since there is practically no comprise in impurity concentration in the bulk of the body region **50**, the encroachment problem of the depletion layer in not much of a concern. With prudent design, the body diffusion curve **66** can be appropriately truncated such that the threshold voltage V_{th} can be maintained to an acceptable level, yet at the same time, the channel length L can be shortened so as to reduce the drain-to-source resistance R_{DS}.

In the preferred embodiment, the truncated body diffusion curve **66** is accomplished by a series of implantation steps. Shown in FIG. **5** is the resultant impurity concentration profile represented by a compensation curve **70** which in essence is a superimposition of three individual implantation curves **70A–70C**. The penetration distances of the individual implantation x=a, x=b, and x=c are first determined. The process of ion implantation is employed to place various dosages of dopant into the substrate **34**. An exemplary technique for implanting a dopant at a predetermined penetration distance into a silicon substrate can be found in a publication by Wolf et al., "Silicon Processing for the VLSI Era", Lattice Press, IEEE Transactions on Electron Devices, Vol. 1, pages 285–291.

FIG. **6** shows a graphical representation of the relationship between the penetration distance and the required energy implantation energy level. For example, in this embodiment, boron (B) is used as the implant material. As an illustration, suppose a distance of 0.3 μ of penetration distance beyond the planar surface **36** (FIG. **3**) is intended. Once the desired penetration distance 0.3 μ is located at the ordinate axis of FIG. **6**, the corresponding value on the abscissa axis can be extracted. As shown in FIG. **6**, the required energy level for the implanting boron is 83 KeV. In a similar manner, positioning implant materials at other penetration distances can likewise be determined. The process of fabricating the semiconductor structure **32** with the aforementioned compensation will be described in more detail hereinafter. It should be noted that in the preferred embodiment, the compensation material is P-type material such as boron which requires less implant energy as compared to other N-type counterparts such as phosphorous or arsenic, as is shown in FIG. **6**.

FIGS. **7A–7M** are sequential views showing the process making the MOSFET device of the invention. In the preferred method, the fabrication process starts with providing a P-type base silicon wafer **54** with a <0.0.1> crystal orientation and a resistivity of between 0.01 Ω-cm=0.02 Ω-cm, for example, as shown in FIG. **7A**. An epitaxial layer **52** with a resistivity of approximately between 0.1 Ω-cm= 5.0 Ω-cm is then grown atop the base wafer **52** to a thickness of approximately 3 to 20 μm. The resultant structure up to this step is shown in FIG. **7B**.

A photoresist layer **72** is then spunned atop the epitaxial layer **52**. Conventional techniques of masking and etching are employed to selectively open windows **74** in the photoresist layer **72**. Using the photoresist **72** as a shielding mask, the structure is then subjected to the standard technique of dry anisotropic etching by exposing the structure to a plasma (not shown) for the formation of the trenches **38** as shown in FIG. **7C**.

What follows is the step of forming gate oxide layers by lining the trenches **38** with insulating material. First, the trenches **38** has to undergo a sacrificial oxidation process. Basically, the structure is exposed to oxidation agent of either oxygen (O_2), if the dry method is employed, or steam (H_2O), if the wet method is preferred, under an ambient temperature of approximately between 90° C.–1,100° C. The grown sacrificial oxide layer **76** is then lightly etched away for the purpose of securing a smooth silicon surface as a prelude for subsequent gate oxide growth. The method of wet etch can be applied for the removal of the sacrificial oxide layer **76**. The finished structure up to this step is shown in FIG. **7D**.

The step of gate oxide growth is then carried out by exposing the structure to either dry or wet agents as described above, under an ambient temperature of between 800° C.–1,100° C. to a thickness of approximately 200 Å–1000 Å. The finished structure with a grown gate oxide layer **44** is shown in FIG. **7E**.

The trenches **38** need to be filled with conductive material. In the preferred method, the trenches **38** are filled with polycrystalline silicon **42** by the conventional method of chemical vapor deposition (CVD). The step of either mechanical or chemical planarization then follows. The remaining polycrystalline silicon **42** is then doped with phosphorus oxychloride ($POCl_3$) to a sheet resistivity of approximately 20–40 Ω/□ under an ambient temperature of about 950° C. The remaining polycrystalline silicon **42** is further chemically etched until the surface is barely below the oxide layer **44** as shown in FIG. **7F**.

It should be noted that the polycrystalline silicon **42** is preferably doped to a N-type conductivity. As is known in the art, the charge carries for N-type material are electrons which have higher mobility than the P-type material counterparts which are holes. Thus, use of N-type polycrystalline

silicon **42** can provide faster turn-on or turn-off time for the MOSFET device. The main reason stems from the reduction in the resistance component of the RC time constant, where R is the distributed resistance and C is the distributed capacitance of any signal propagation path. However, doping the polycrystalline gate to N-type in a P-channel MOSFET device always results in a high threshold voltage, as is the case with most prior art processes. The method of the present invention is especially advantageous under this situation because the threshold level can be reasonably adjusted to any level without disturbing other parameters of the device as explained previously.

Reference is now returned back to FIG. **7**G. Another photoresist mask **78** is patterned above the structure, which is then ion-implanted with phosphorous (P) under an implant potential of approximately 60 KeV–100 KeV at a dosage of about 2×10^{13} cm^{-2} to 2×10^{14} cm^{-2}. It should be noted that the photoresist mask **78** is used mainly for the fabrication of the termination circuits (not shown) and its use for the processing of the MOSFET cell **46** is optional. Without the mask **78**, phosphorous ions can well be implanted into the polycrystalline silicon **42** as it has already been doped heavily with the N-type dopant ($POCl_3$) as described above. The heavily doped N-type dopant overshadows the relatively lightly doped phosphorous in the polycrystalline silicon **42**. The photoresist mask **78**, if used as shown in FIG. **7**G, is then stripped away from the structure which then undergoes a drive-in cycle at a temperature of about 1,000° C.–1,200° C., resulting in a lightly doped N-type body layer **50** driven in the epitaxial layer **52** as shown in FIG. **7**H.

Thereafter the deposition of the source layer **48** follows. First, the remnant surface oxide is removed. Another photoresist mask **86** with source layer windows **88** is then formed on the top of the structure. Boron is then ion-implanted into the masked structure with an implant dosage of approximately 5×10^{15} cm^{-2} to 1×10^{16} cm^{-2} under an implant potential of between 40 KeV to 100 KeV, as shown in FIG. **7**I.

The step of body region compensation is the next step in the fabrication process. Reference is now directed back to FIGS. **3**–**5**. To secure a reasonably level body diffusion curve **66** near the body junction $x=x_{js}$, successive implantations at various distances from the planar surface **36** (FIG. **3**) are preferred. It this method, boron ions are implanted at distances of x=a, x=b and x=c from the planar surface **36** (FIG. **3**), which distances correspond to the individual implant profiles **70**A, **70**B and **70**C, respectively, as shown in FIG. **5**. Profile **70**B can be higher in amplitude and can be coincident with the peak value of the body diffusion curve **66** had the curve **66** not been compensated (that is, the uncompensated curve **30**). Once the distances x=a, x=b and x=c are determined, the corresponding implant energy levels can be extracted from the energy chart as shown in FIG. **6**. Boron is then driven into the structure as shown in FIG. **7**J by the process of ion-implantation in which implant dosages are set by the implant durations.

In the preferred method, the source implant and the compensation implant are subjected to a combined drive-in cycle under a temperature of between 900° C.–1,000° C. for a duration of between 10 minutes to 2 hours. The resultant structure with the deposited source layer **48** and the compensated body region **50** is shown in FIG. **7**K.

After the drive-in cycle, the resultant implant profile is essentially an envelope curve **70** encompassing all the individual profiles **70**A–**70**C. The compensation curve **70** of FIG. **5** when superimposed with the pre-compensated diffusion profile as shown in FIG. **4** results in the body diffusion curve **66** with reduced impurity concentration near the source junction $x=x_{js}$, as compared to the pre-compensated profile **30** where there is no such reduction. As mentioned before, the ordinate axis of FIG. **4** is shown in logarithm scale and the reduction in impurity concentration near the source junction $x=x_{js}$ is in fact a substantial amount. Moreover, the reduction in impurity concentration is remote from the body boundary $x=x_{jb}$ where the depletion region **24** originates and extends. Since there is no comprise in impurity concentration adjacent to the body boundary at $x=x_{jb}$, the encroachment problem of depletion layer **24** into the source region **48** would not be a concern.

Thereafter, the deposition steps of the passivation layer **56** follows. The material for the passivation layer **56** can be phosphosilicate glass (PSG). Afterwards, another photoresist layer **82** is then formed atop the passivation layer **56**. The photoresist layer **82** is then patterned with contact windows **84** as shown in FIG. **7**L.

The passivation layer **56** is etched through the patterned mask **82** using an etchant which significantly attacks the passivation layer **56** but not the patterned photoresist mask **82**. Either the method of dry etch or wet etch can be employed. If the dry etch method is used, the etchant is plasma. If the wet etch method is adopted, the etchant can be HF. Thereafter, the mask **82** is removed, the resultant structure up to this step is shown in FIG. **7**M.

Utilizing the patterned passivation layer **56** as a mask, phosphorous ions are then implanted into the structure as shown in FIG. **7**M. The implanted phosphorous is thereafter driven in the N-type body layer **50** to a slight depth. Consequently, contact regions **80** are formed in the substrate **34** as will be shown in FIG. **7**N.

The passivation layer **56** is then subjected to a densification process under a temperature range of about 900° C.–950° C. for 30 minutes to 60 minutes. After the densification process, the corners of the passivation layer **56** are rounded off. The source and drain metal contact layers **58** and **60** can thereafter be deposited with conventional microelectronic processing techniques and are not further elaborated in here. The eventual structure up to this step is shown in FIG. **7**N.

Finally, other changes are possible within the scope of the invention. The source implantation step shown in FIG. **7**I and the body region compensation implantation step shown in FIG. **7**J can well be reversed. That is, it is perfectly possible to perform the compensation implantation step prior to the source implantation step. Furthermore, the source implant resulted from the implantation step shown in FIG. **7**I, and the compensation implant resulted from the implantation step shown in FIG. **7**J can assume separated drive-in cycles. As mentioned before, the conductivity types of the layers may very well be different from that as depicted in the specification. In the preferred embodiment, the semiconductor structure is a P-channel MOSFET device. The structure can well be built as a N-channel device. Furthermore, the portion of the body region adjacent to the source need not be fully compensated with a dopant of opposite conductivity type. A partially compensated body region can well result in a MOSFET device with a reduced threshold voltage. In addition, the device fabricated in accordance with the invention need not be a power MOSFET. It can well be slightly modified and used for other purposes, such as a dynamic random access memory (DRAM) cell, an insulated gate bipolar transistor (IGBT), or a charge-coupled-device (CCD), to name just a few. It will

be understood by those skilled in the art that these and other changes in form and detail may be made therein without departing from the scope and spirit of the invention.

What is claimed is:

1. A method of forming a semiconductor structure comprising the steps of:

(a) providing a substrate having a major surface;

(b) forming at least one trench in said substrate;

(c) forming a body region of a first conductivity type in said substrate, said body region having a diffusion boundary in said substrate;

(d) forming a source region of a second conductivity type in said body region; and

(e) compensating a portion of said body region by implanting material of said second conductivity type in said body region, said portion being proximal to said source region and spaced from said diffusion boundary of said body region and said major so as to reduce the impurity concentration of said first conductivity type in said portion of said body region.

2. The method of forming a semiconductor structure as set forth in claim 1 further including filling said at least one trench with N-type material.

3. The method of forming a semiconductor structure set forth in claim 1 wherein step (a) includes providing a base substrate of said second conductivity type and forming an epitaxial layer of said second conductivity type above said base substrate.

4. The method of forming a semiconductor structure as set forth in claim 1 wherein step (c) includes the substeps of ion implanting material of said body region in said substrate and thereafter diffusing said material of said body region in said substrate.

5. The method of forming a semiconductor structure as set forth in claim 1 wherein step (d) includes the substeps of ion implanting material of said source region in said substrate and thereafter diffusing said material of said source region in said body region.

6. The method of forming a semiconductor structure as set forth in claim 5 wherein step (e) includes ion implanting material of said second conductivity type in said body region at a predetermined distance from said source region.

7. The method of forming a semiconductor structure as set forth in claim 5 wherein step (e) includes successive substeps of ion implanting material of said second conductivity type in said body region at predetermined distances from said source region.

8. The method of forming a semiconductor structure as set forth in claim 1 wherein step (e) is performed prior to step (d).

9. The method of forming a semiconductor structure as set forth in claim 1 further comprising the step of simultaneously diffusing said source region and said compensated portion of said body region after step (e).

10. The method of forming a semiconductor structure as set forth in claim 1 further comprising forming a gate region formed of material of N-type conductivity dielectrically separated from said body region.

11. The method of forming a semiconductor structure as set forth in claim 1 wherein said first conductivity type is of N-type and said second conductivity is of P-type.

12. The method of forming a semiconductor structure as set forth in claim 1 wherein the implanting material in step (e) is boron.

13. A method of forming a semiconductor structure having a trench gate with a gate threshold voltage, said method comprising the steps of:

(a) providing a substrate having a major surface;

(b) forming a body region of a first conductivity type in said substrate, said body region having a diffusion boundary in said substrate;

(c) forming a source region of a second conductivity type in said body region; and

(d) compensating a portion of said body region by implanting material of said second conductivity type in said body region adjacent to said source region and spaced from said diffusion boundary of said body region and said major surface such that the impurity concentration of said portion of said body region is substantially reduced so as to decrease the gate threshold voltage of said trench gate.

14. The method of forming a semiconductor structure as; set forth in claim 13 wherein step (d) is performed prior to step (c).

15. The method of forming a semiconductor structure as set forth in claim 13 wherein step (d) includes ion implanting material of said second conductivity type in said body region at a predetermined distance from said source region.

16. The method for forming a semiconductor structure as set forth in claim 15 wherein step (d) further including diffusing said compensated portion of said body region in said body region.

17. The method of forming a semiconductor structure as set forth in claim 13 wherein step (d) includes successive substeps of ion implanting material of said second conductivity type in said body region at predetermined distances from said source region.

18. The method of forming a semiconductor structure as; set forth in claim 17 further including the substep of filling said at least one trench with N-type material.

19. The method of forming a semiconductor structure as set forth in claim 18 wherein step (b) includes the substeps of ion implanting material of said body region in said substrate and thereafter diffusing material of said body region in said substrate.

20. The method of forming a semiconductor structure as set forth in claim 19 wherein step (c) includes the substeps of ion implanting material of said source region in said substrate and thereafter diffusing material of said source region in said body region.

21. The method of forming a semiconductor structure as set forth in claim 19 wherein step (d) includes the substep of diffusing the compensated portion of said body region in said body region and wherein the diffusing of said source region and the diffusing of said compensated portion of said body region are performed simultaneously.

22. The method of forming a semiconductor structure as set forth in claim 21 wherein step (a) includes the substeps of providing a base substrate of said second conductivity type and forming an epitaxial layer of said second conductivity type above said base substrate.

23. The method of forming a semiconductor structure as set forth in claim 22 wherein said first conductivity type is of N-type and said second conductivity is of P-type.

24. The method of forming a semiconductor structure as set forth in claim 23 wherein the implanting material in step (d) is boron.

25. A method of forming a semiconductor structure having a gate with a gate threshold voltage, said method comprising the steps of:

(a) providing a substrate having a major surface;

(b) forming at least one trench in said substrate extending from said major surface;

(c) forming a body region of a first conductivity type in said substrate to a diffusion boundary extending from said major surface;

(d) forming a source region of a second conductivity type in said body layer extending from said major surface; and

(e) compensating a portion of said body region by implanting material of said second conductivity type in said body region adjacent to said source region and spaced from said diffusion boundary of said body layer and said major surface such that the conductivity of said portion of said body region is substantially reduced so as to decrease the gate threshold voltage of said gate.

26. The method of forming a semiconductor structure as set forth in claim **25** wherein step (b) includes the substep of lining said trenches with insulating material and followed by another substep of filing said trenches with conductive material.

27. The method of forming a semiconductor structure as set forth in claim **26** wherein said conductive material is a N-type material.

28. The method of forming a semiconductor structure as set forth in claim **25** wherein step (e) includes ion implanting material of said second conductivity type in said body region at a predetermined distance from said source region.

29. The method of forming a semiconductor structure as set forth in claim **25** wherein step (e) includes successive substeps of ion implanting material of said second conductivity type in said body region at predetermined distances from said source region.

* * * * *

EXHIBIT 5

US005930630A

United States Patent [19]

Hshieh et al.

[11] **Patent Number: 5,930,630**

[45] **Date of Patent: Jul. 27, 1999**

[54] **METHOD FOR DEVICE RUGGEDNESS IMPROVEMENT AND ON-RESISTANCE REDUCTION FOR POWER MOSFET ACHIEVED BY NOVEL SOURCE CONTACT STRUCTURE**

[75] Inventors: **Fwu-Iuan Hshieh**, Saratoga; **Kong Chong So**; **Danny Chi Nim**, both of San Jose, all of Calif.

[73] Assignee: **MegaMOS Corporation**, San Jose, Calif.

[21] Appl. No.: **08/899,186**

[22] Filed: **Jul. 23, 1997**

[51] **Int. Cl.**[6] **H01L 21/336**

[52] **U.S. Cl.** **438/268**; 438/307

[58] **Field of Search** 438/138, 156, 438/268, 273, 307, 529, 545

[56] **References Cited**

U.S. PATENT DOCUMENTS

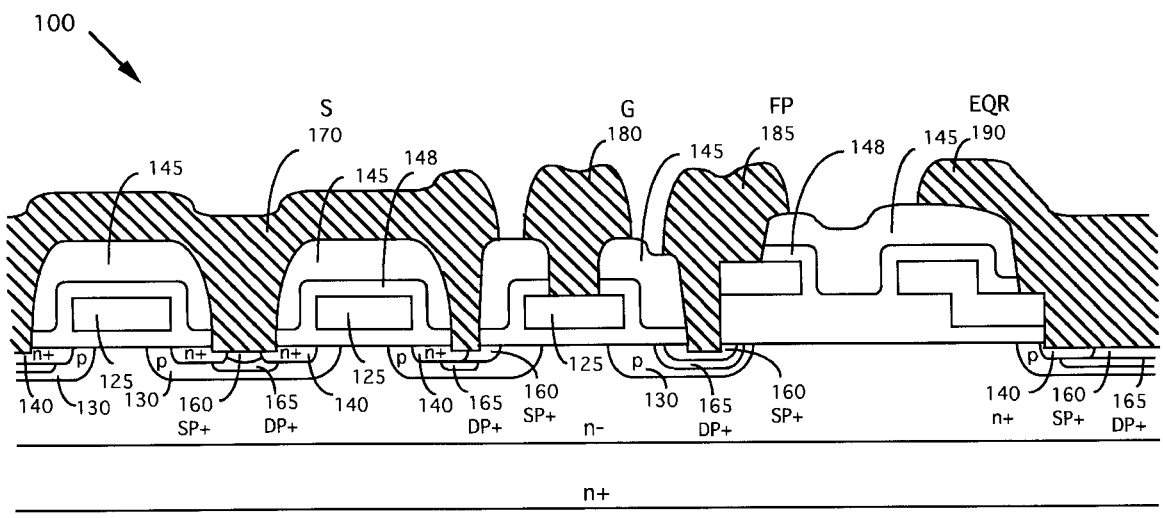
5,119,153	6/1992	Korman et al.	257/341
5,250,449	10/1993	Kuroyanagi et al.	438/268
5,286,586	2/1994	Mukherjee et al.	257/341
5,460,986	10/1995	Tam et al.	438/268
5,663,079	9/1997	Blanchard	438/268

Primary Examiner—Chandra Chaudhari
Attorney, Agent, or Firm—Bo-In Lin

[57] **ABSTRACT**

The invention discloses method for fabricating a MOSFET on a substrate to improve device ruggedness. The method includes steps of: (a) forming an epi-layer of a first conductivity type as a drain region on the substrate and growing an initial oxide layer over the epi-layer; (b) applying an active mask for etching the active layer to define an active area followed by depositing an overlaying polysilicon layer and applying a polysilicon mask for etching the polysilicon layer to define a plurality of polysilicon gates; (c) removing the mask and carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions; (d) applying a source blocking mask for implanting a plurality of source regions in the body regions with ions of the first conductivity type followed by removing the blocking mask and a source diffusion process; (e) forming an overlying insulation layer covering the MOSFET followed by applying a contact mask to open a plurality of contact openings; (f) performing a low energy body-dopant and high energy body dopant implant to form a shallow high-concentration body dopant and a deep high-concentration body dopant region followed by applying a high temperature process for densification of the insulation layer and activating diffusion of the deep and shallow body dopant regions wherein the deep high-concentration body-dopant regions are formed below the source regions and extends beyond the contact regions but are kept at lateral distance away from a channel region of the MOSFET in the body region whereby device ruggedness is improved without increasing threshold voltage.

7 Claims, 13 Drawing Sheets



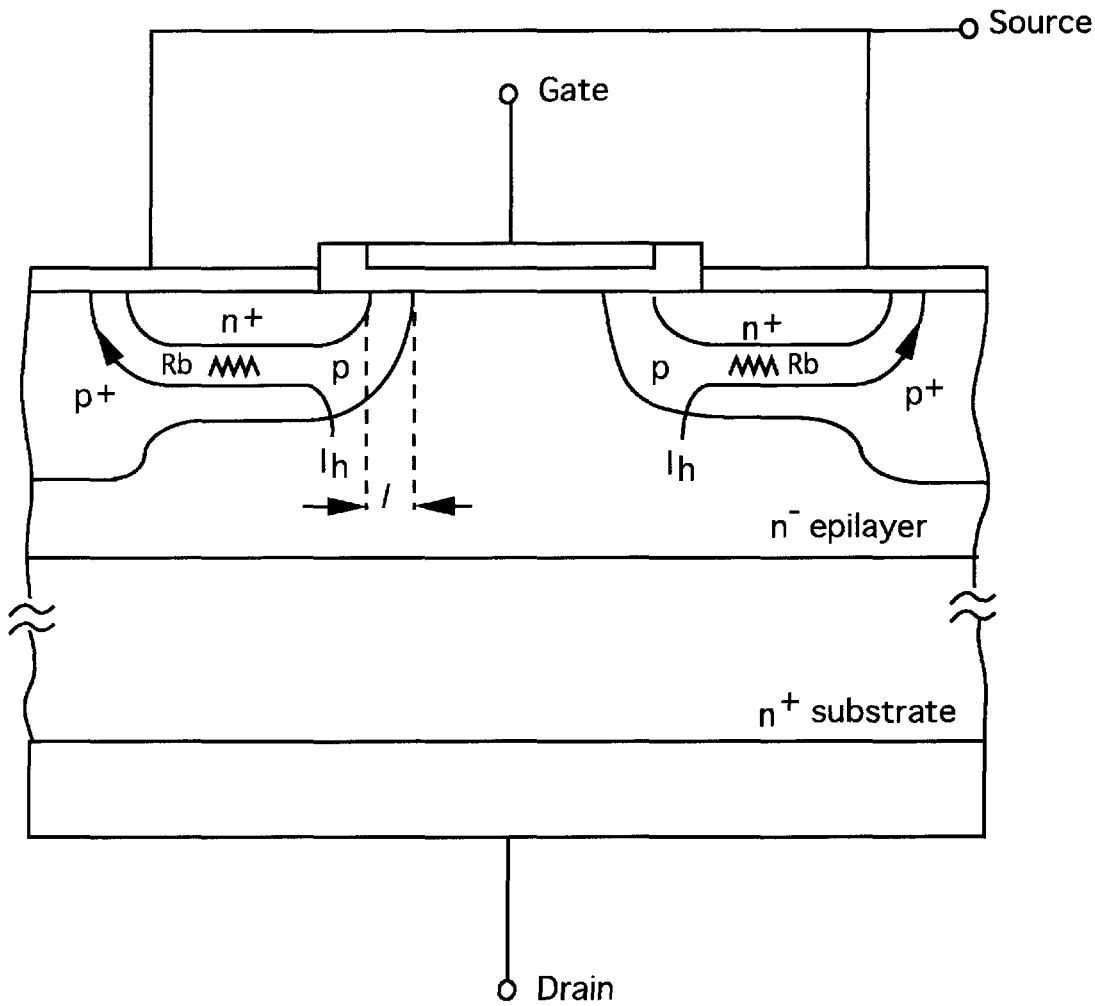


FIG. 1 (Prior Art)

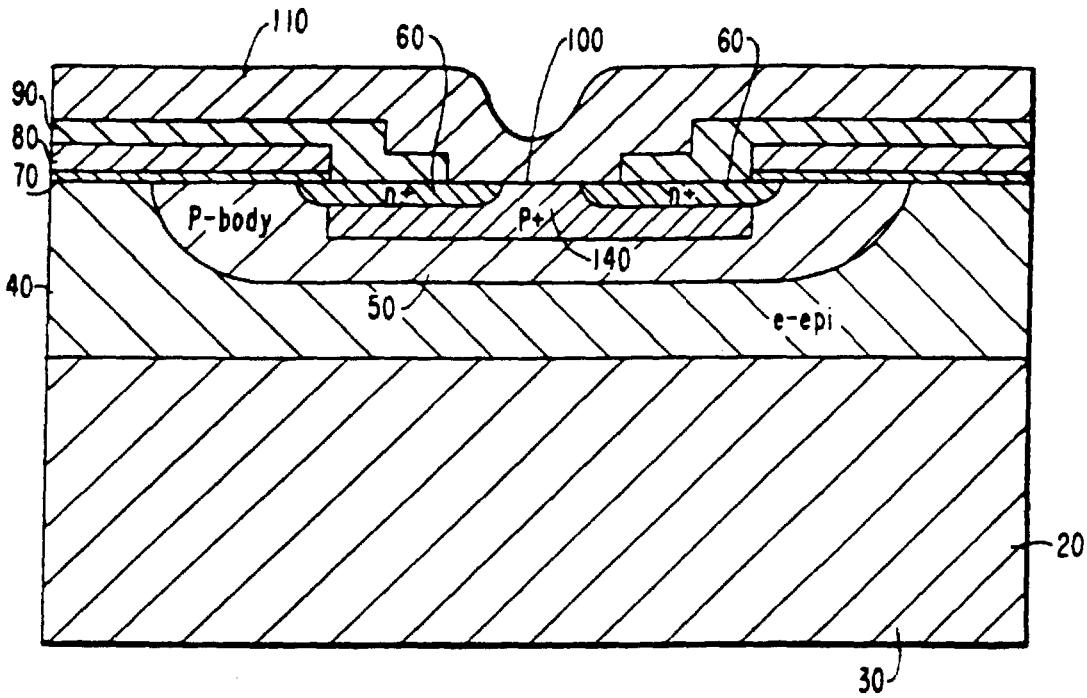


FIG. 2A
(Prior Art)

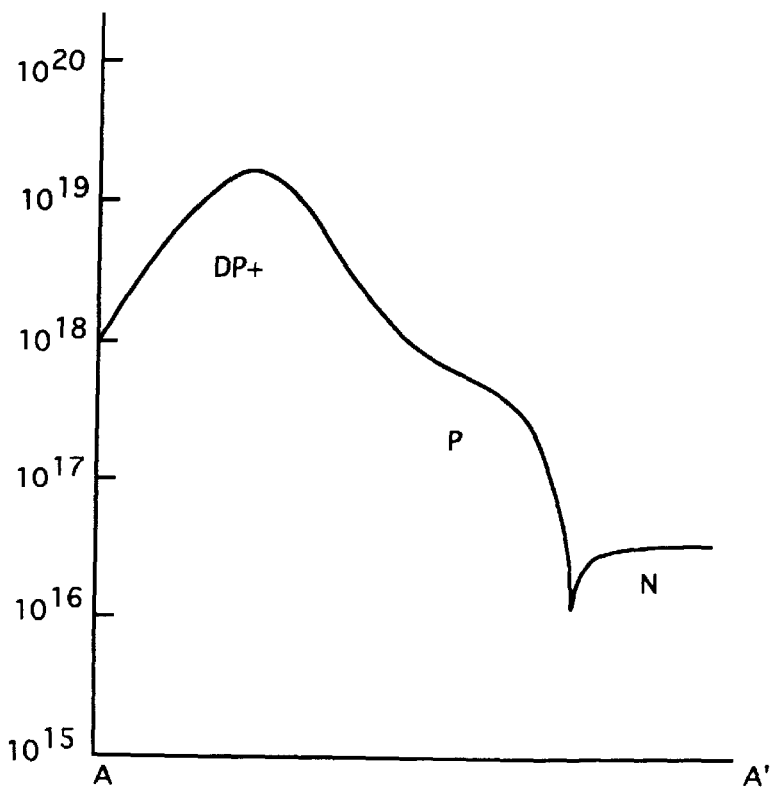


FIG. 2B
(Prior Art)

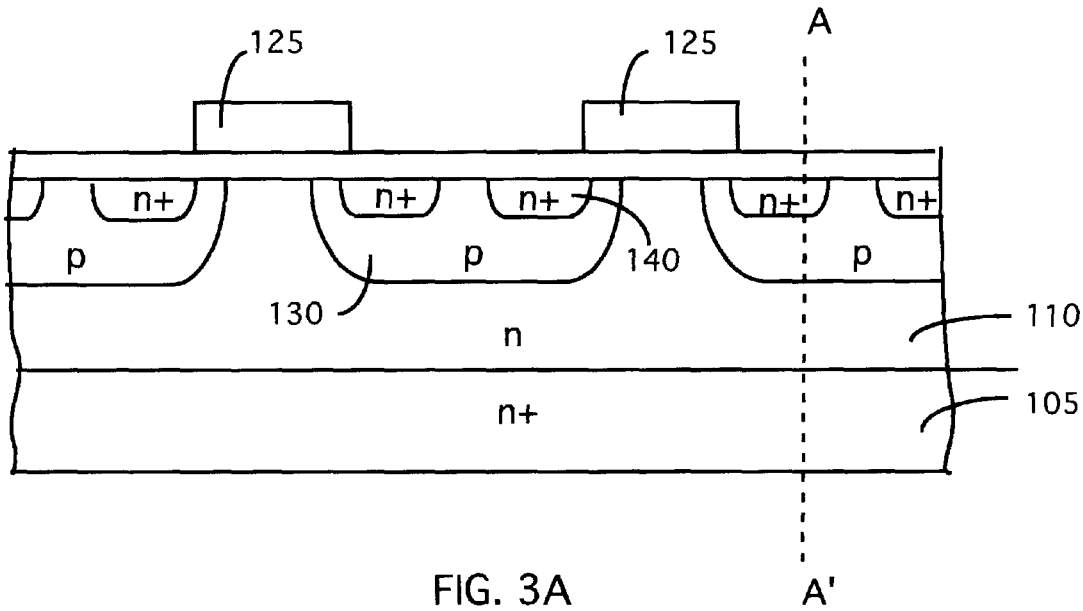

125
125
A
n+
n+
n+
n+
n+
p
p
p
140
130
110
n
n+
105
A'

FIG. 3A

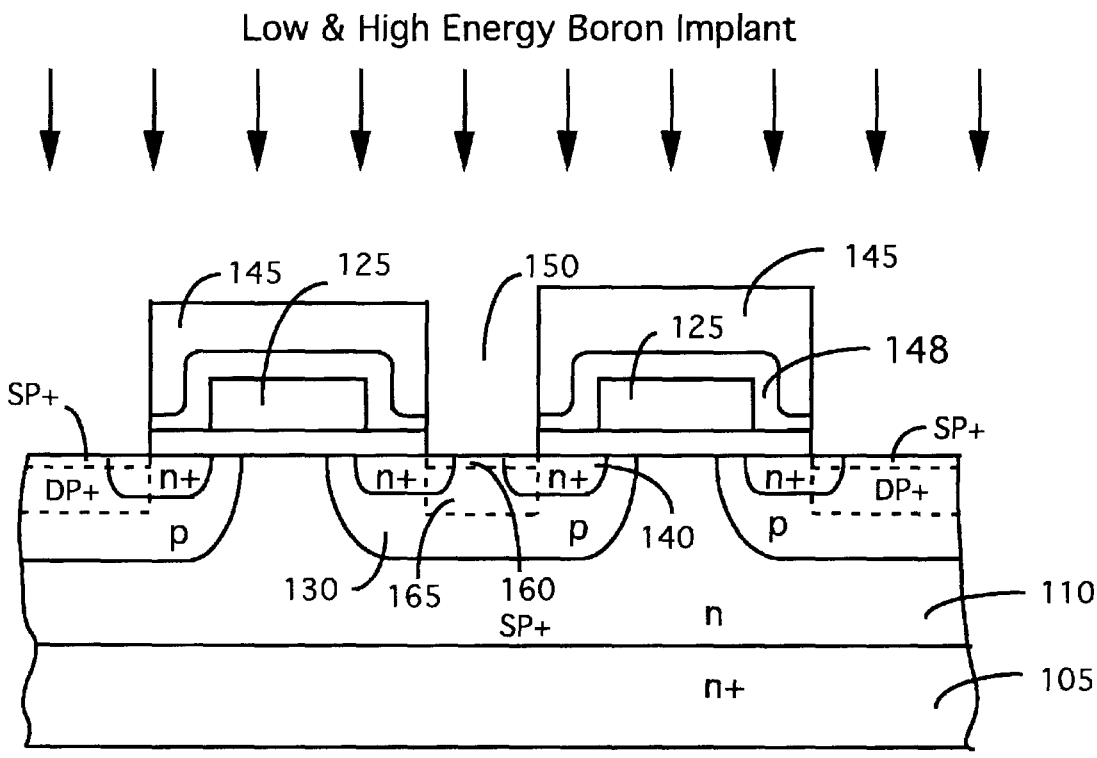

Low & High Energy Boron Implant
145
125
150
145
125
148
SP+
SP+
DP+
n+
n+
n+
n+
DP+
p
p
p
140
130
165
160
SP+
110
n
n+
105

FIG. 3B

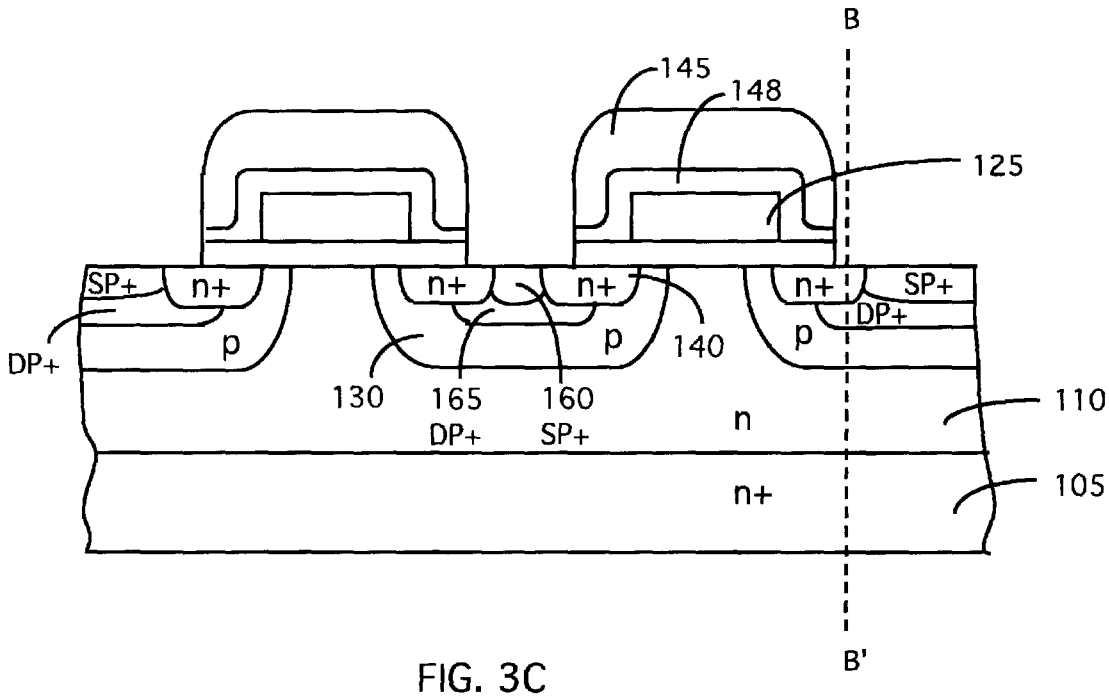

B
145
148
125
SP+
n+
n+
n+
n+
SP+
DP+
DP+
p
p
p
140
130
165
DP+
160
SP+
n
110
n+
105
B'

FIG. 3C

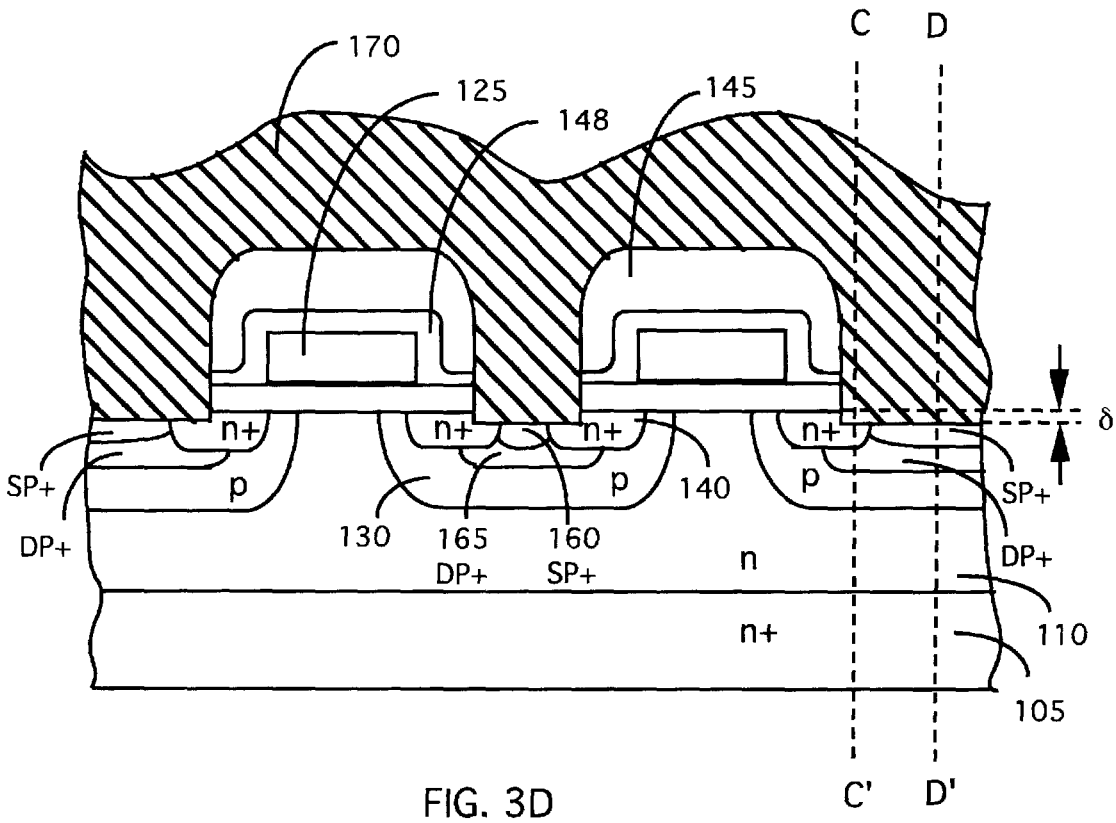

C
D
170
125
148
145
δ
n+
n+
n+
n+
SP+
p
p
p
140
SP+
DP+
130
165
DP+
160
SP+
n
DP+
n+
110
105
C'
D'

FIG. 3D

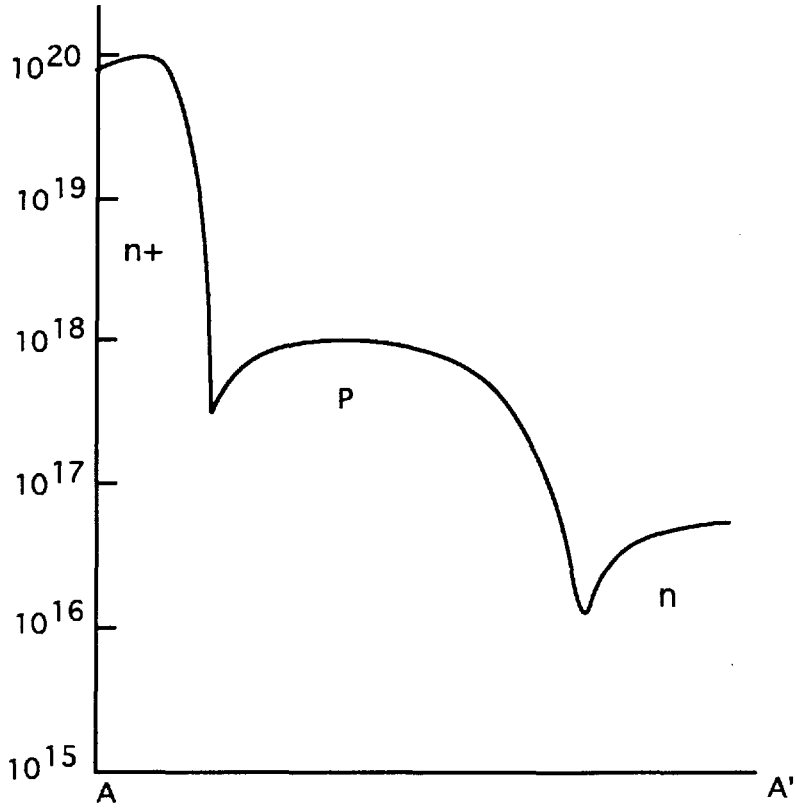

10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
n+
P
n
A
A'

FIG. 4A

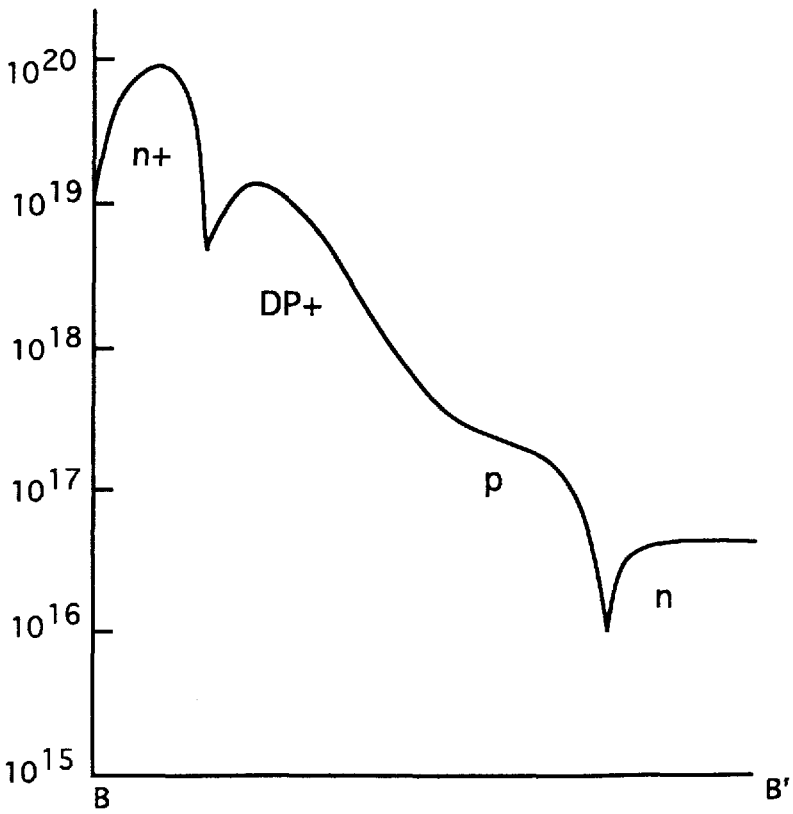

10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
n+
DP+
p
n
B
B'

FIG. 4B

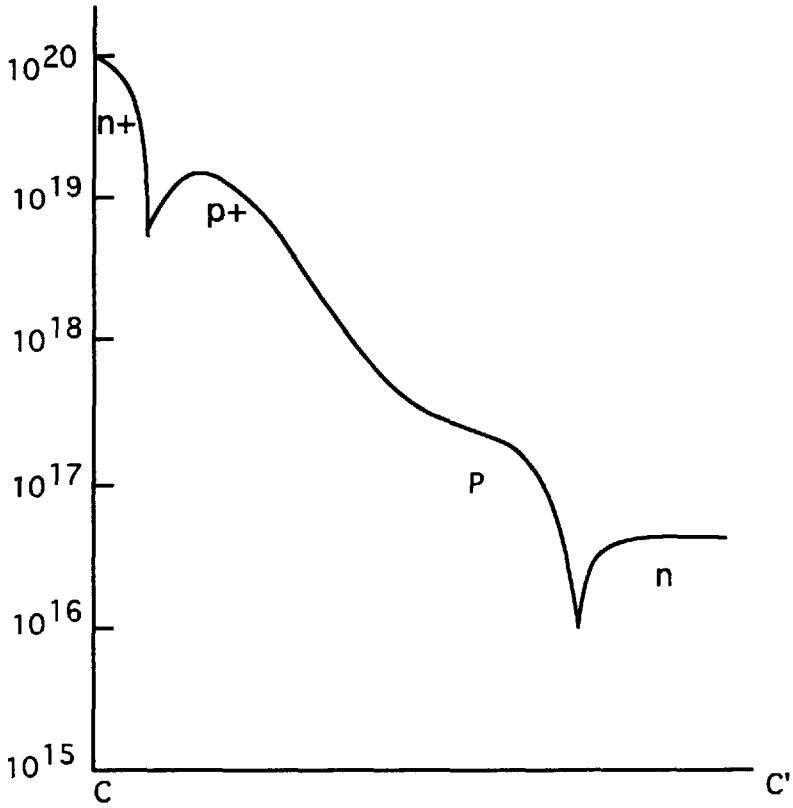

10^{20}
n+
10^{19}
p+
10^{18}
10^{17}
P
n
10^{16}
10^{15}
C
C'

FIG. 4C

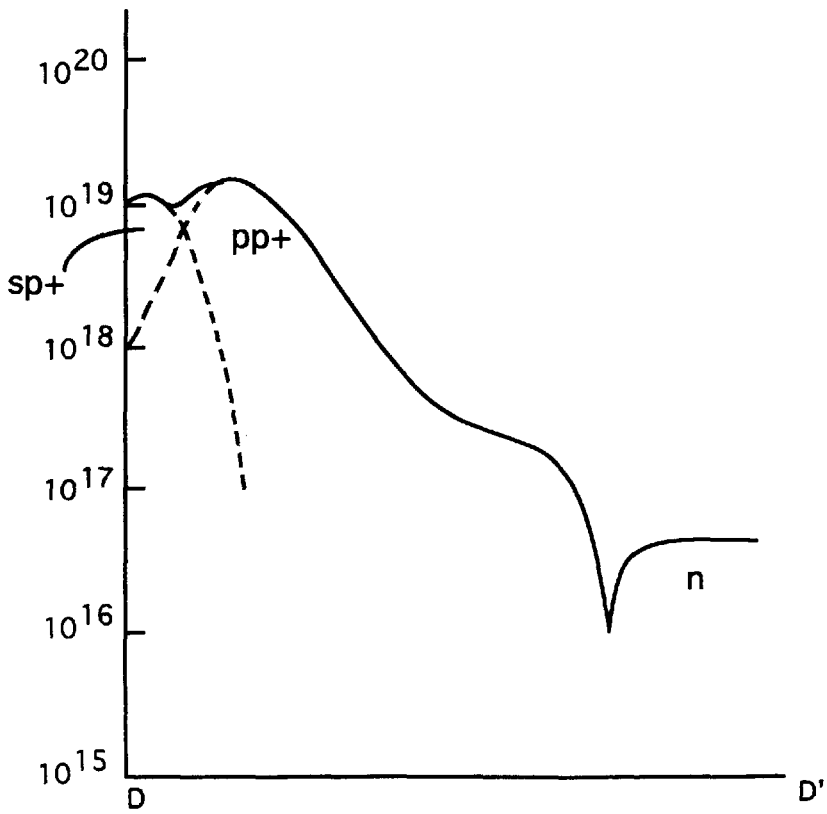

10^{20}
10^{19}
X
pp+
sp+
10^{18}
10^{17}
n
10^{16}
10^{15}
D
D'

FIG. 4D

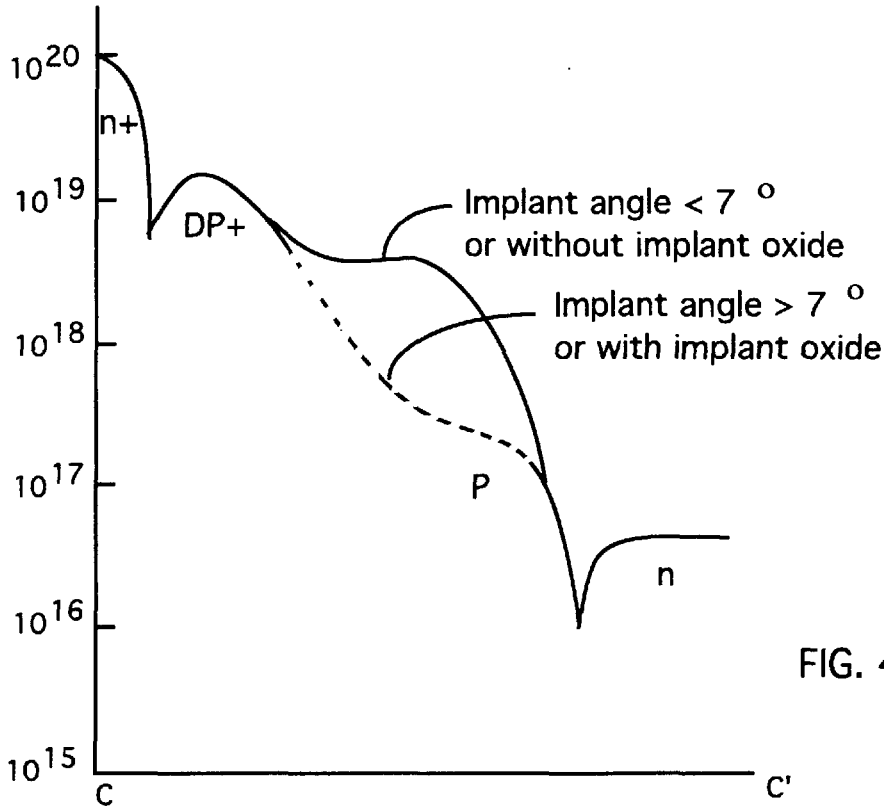

10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
n+
DP+
Implant angle < 7 °
or without implant oxide
Implant angle > 7 °
or with implant oxide
P
n
C
C'

FIG. 4E

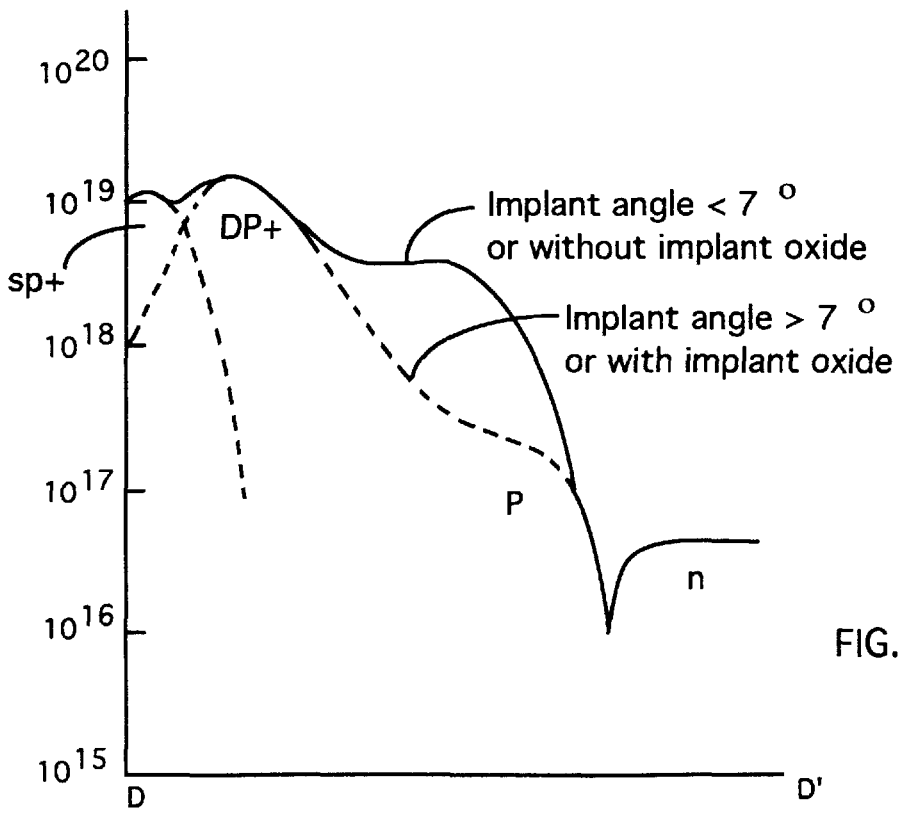

10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
sp+
DP+
Implant angle < 7 °
or without implant oxide
Implant angle > 7 °
or with implant oxide
P
n
D
D'

FIG. 4F

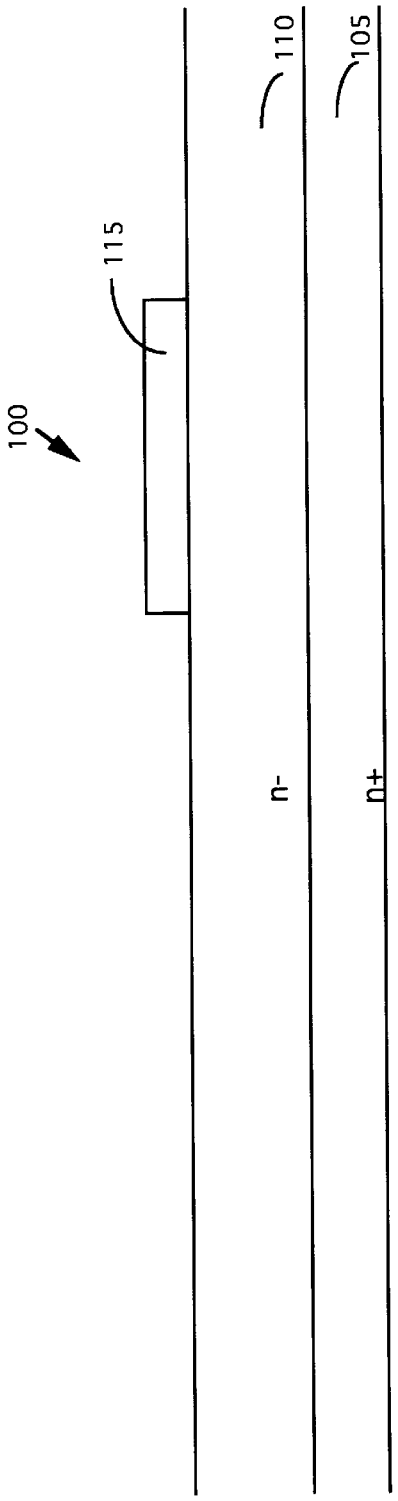


FIG. 5A

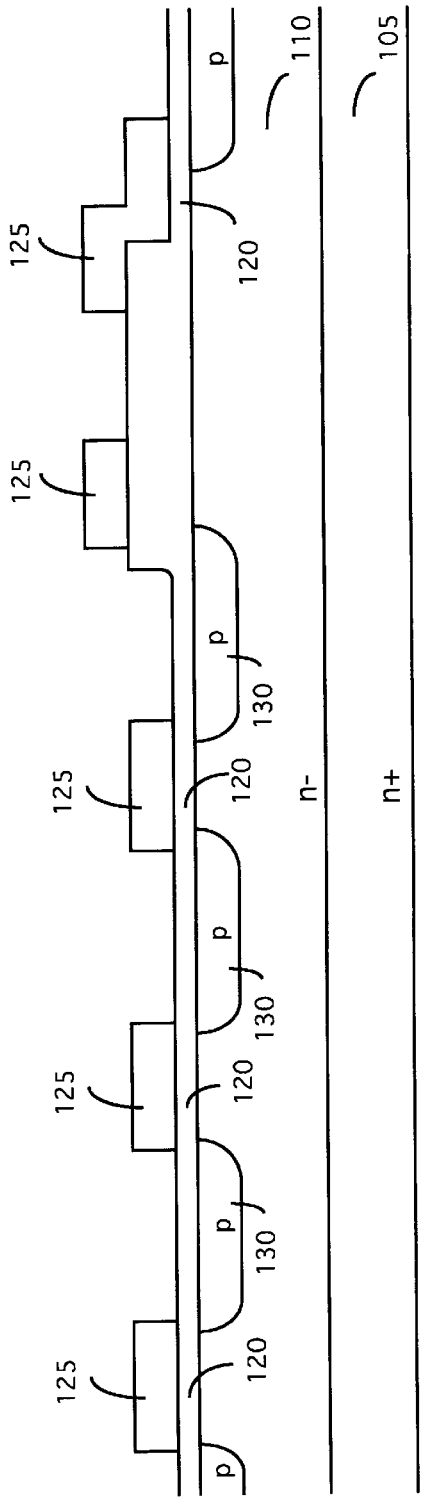


FIG. 5B

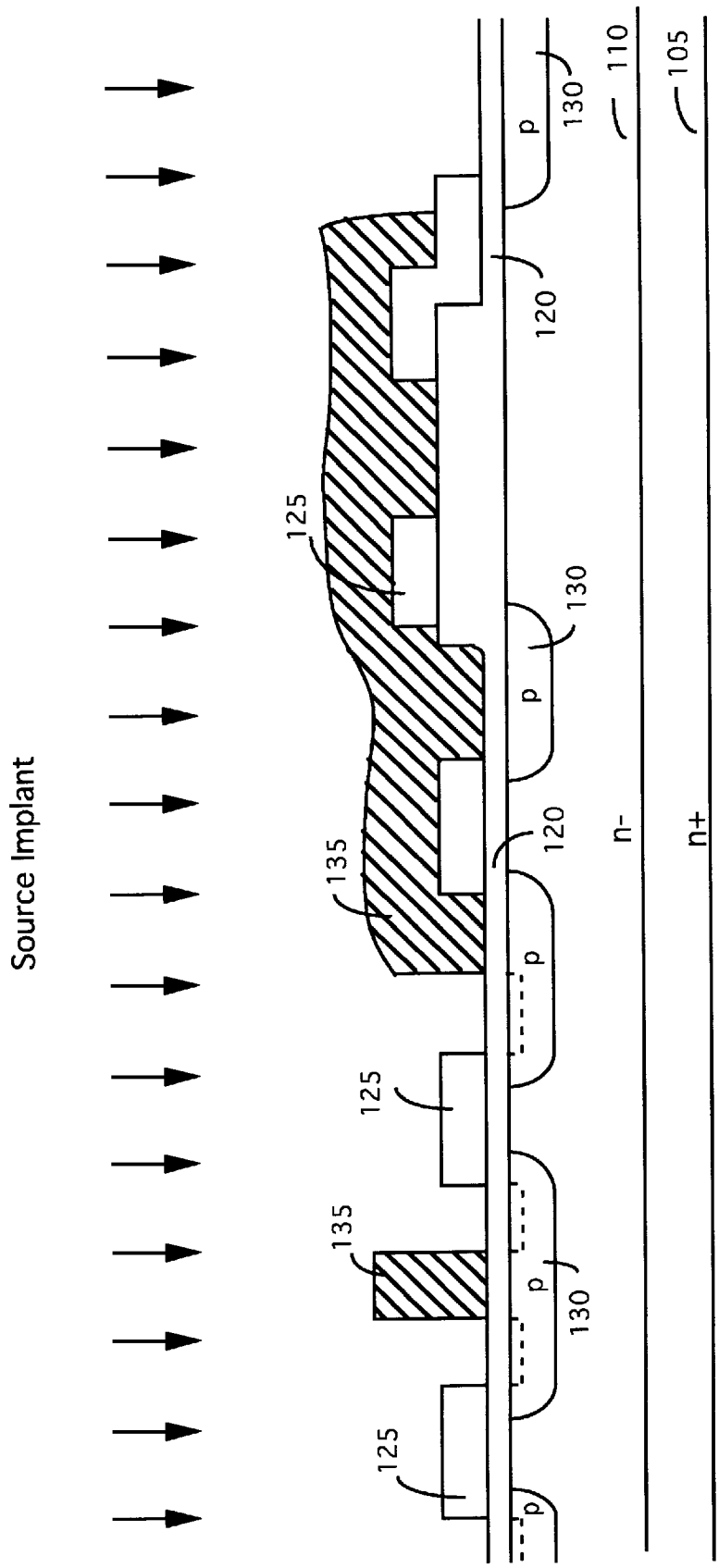

Source Implant
125
135
125
135
125
p
p
p
p
p
p
120
120
130
130
130
110
105
n-
n+

FIG. 5C

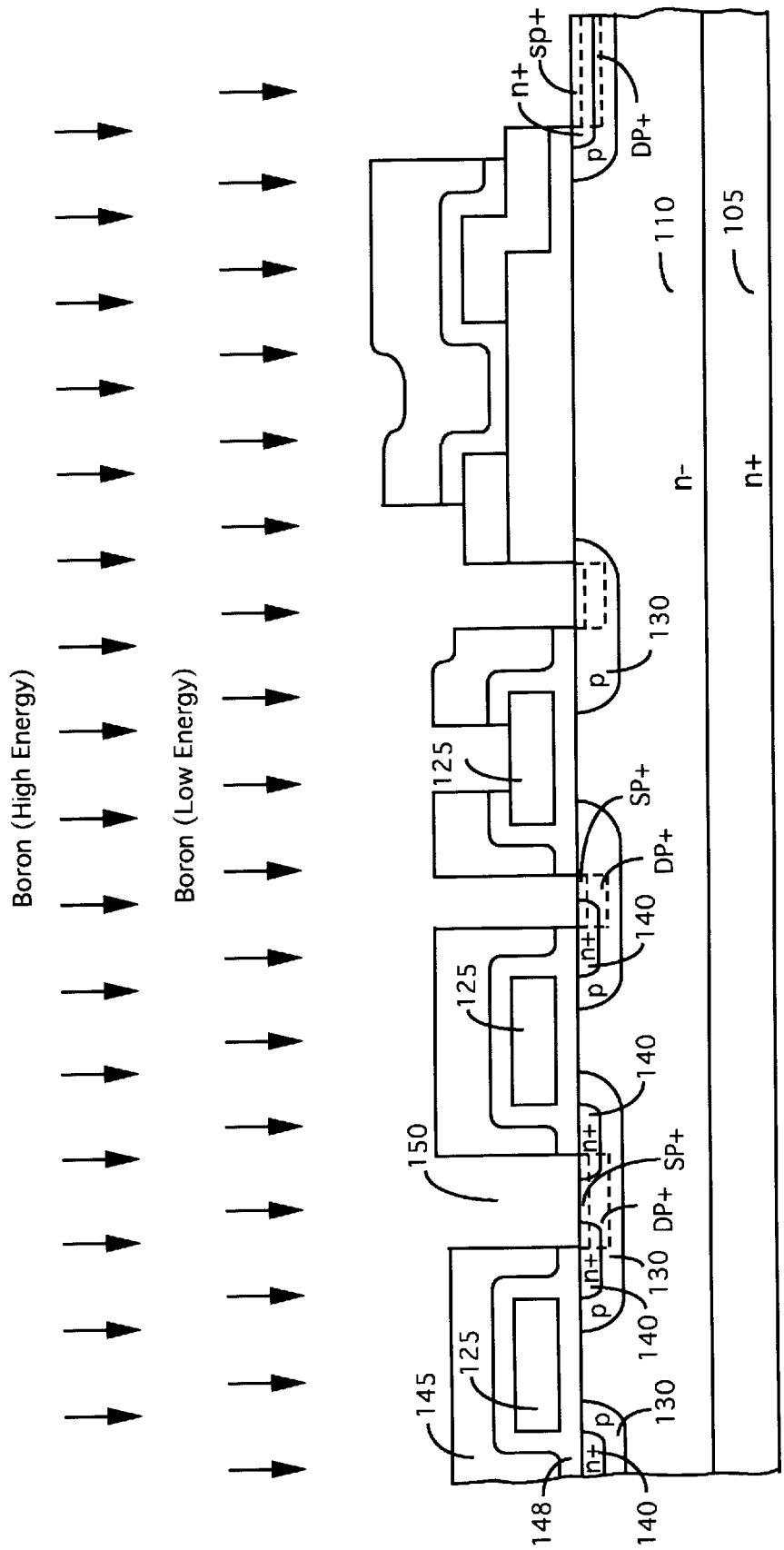

Boron (High Energy)
Boron (Low Energy)
n+
sp+
DP+
110
105
n-
n+
p
130
125
SP+
DP+
140
p
n+
125
140
150
SP+
n+
DP+
130
p
140
125
145
130
p
n+
148
140

FIG. 5D

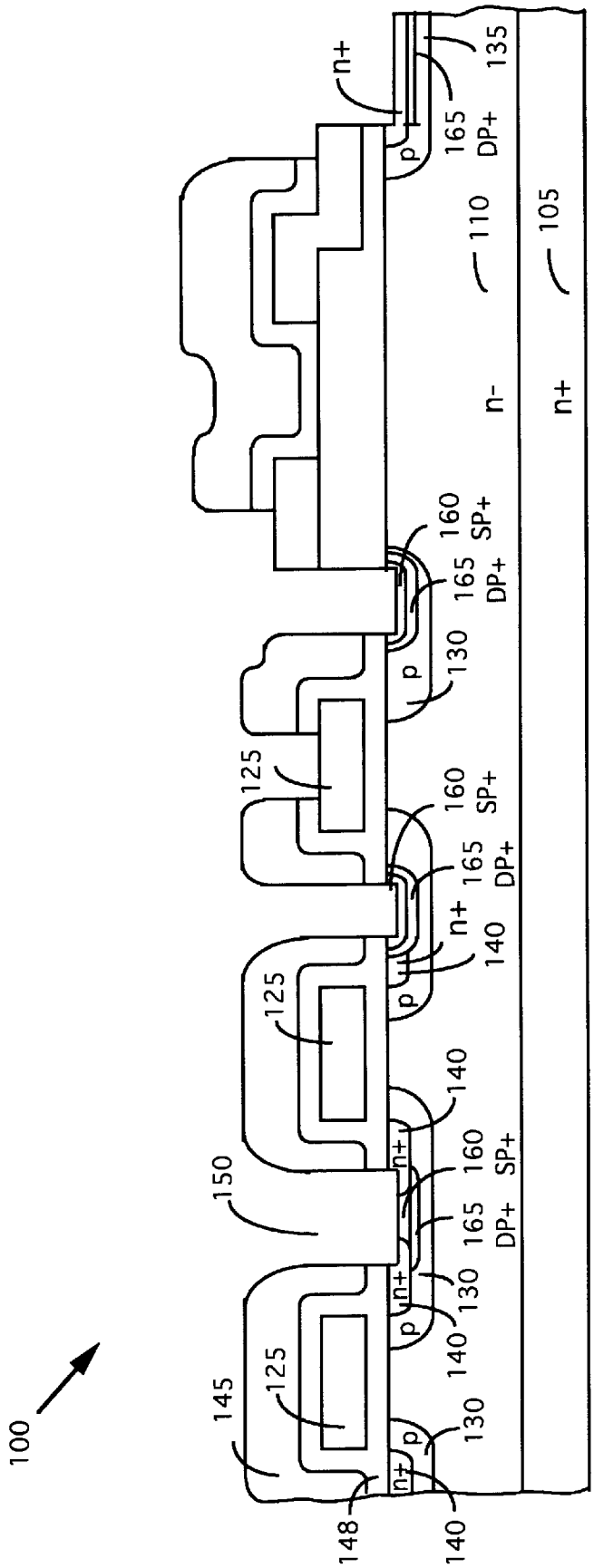

100
145
125
150
125
125
n+
p
n+
p
n+
p
n+
p
n+
p
n+
148
140
130
140
130
140
165
DP+
160
SP+
165
DP+
160
SP+
165
DP+
135
110
105
n-
n+

FIG. 5E

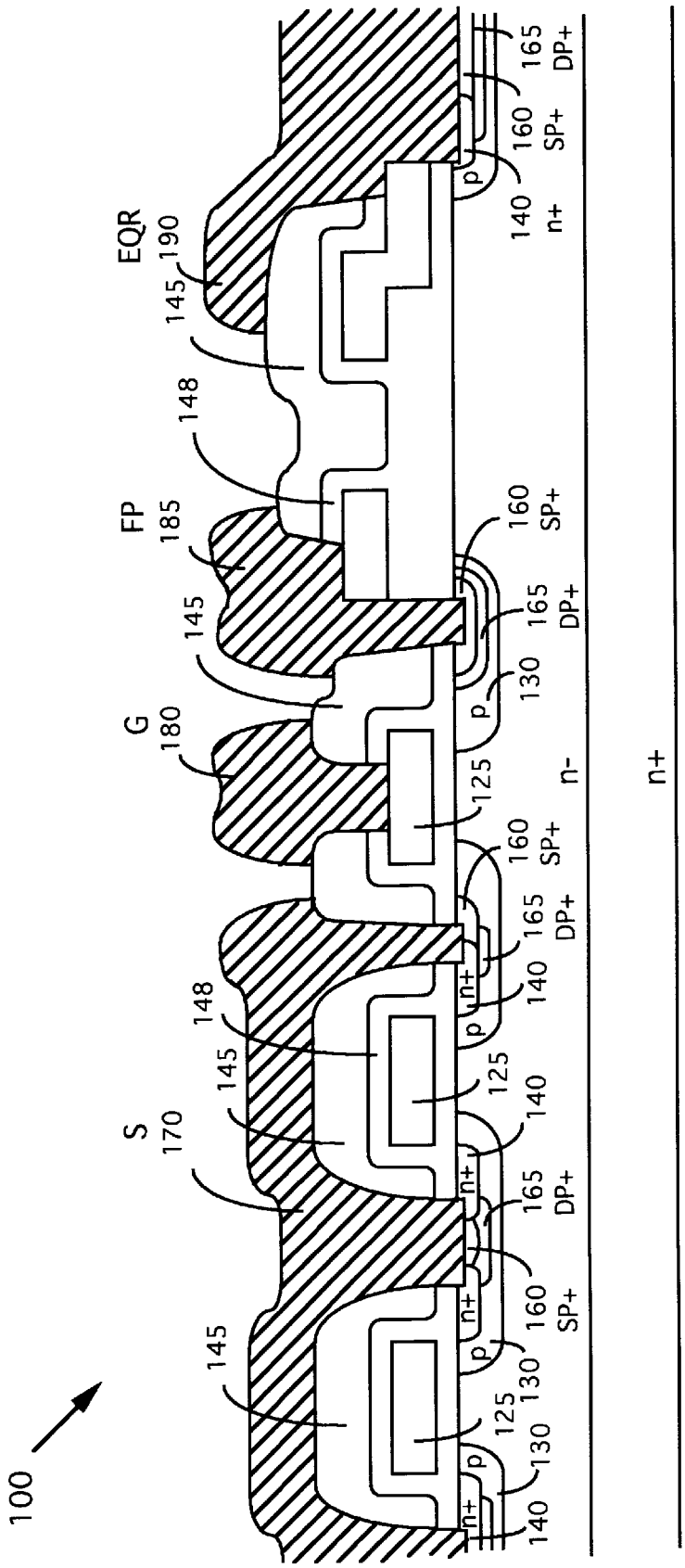

100
EQR
FP
G
S
190
145
148
185
180
170
160
SP+
165
DP+
140
n+
130
125
p
n-

FIG. 5F

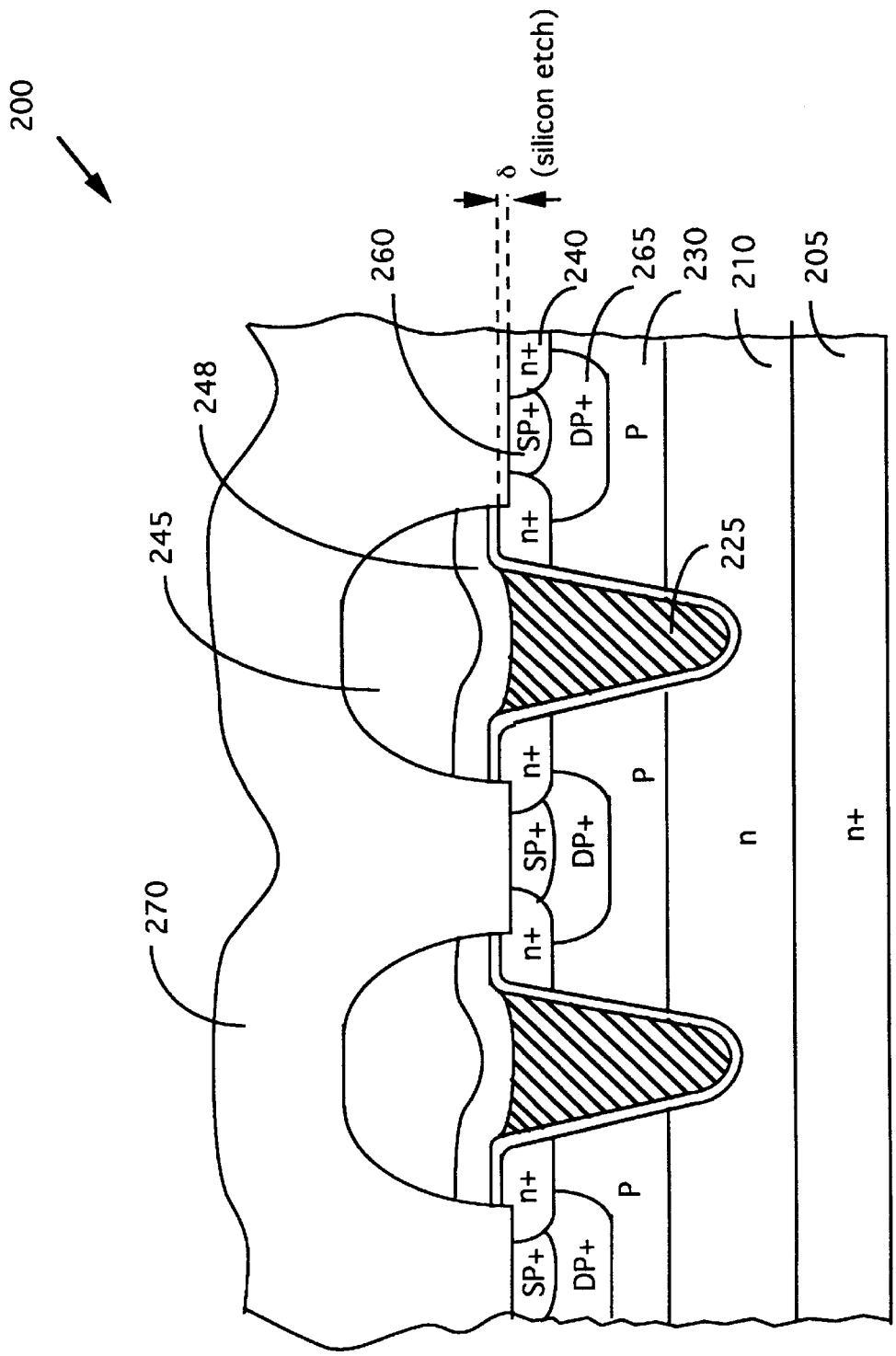

200
δ (silicon etch)
260
240
265
230
210
205
248
245
225
270
n+
SP+
DP+
P
n
n+

FIG. 6

METHOD FOR DEVICE RUGGEDNESS IMPROVEMENT AND ON-RESISTANCE REDUCTION FOR POWER MOSFET ACHIEVED BY NOVEL SOURCE CONTACT STRUCTURE

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to the cell structure and fabrication process of vertical power transistors. More particularly, this invention relates to device ruggedness improvement and on resistance reduction by implementing a novel source contact structure and fabrication process.

2. Description of the Prior Art

For the purpose of improving the device ruggedness, limitations of higher fabrication cost and product reliability concerns still exist in the manufacture of power MOSFET transistors of shallower junctions. In order to achieve higher device ruggedness, a more complicate processes are often applied. These processes involve either the use of an extra implant mask to form a buried body implant region under the source region or the formation of spacer. The gate sidewall spacer is often applied which employs an oxide spacers to form the self aligned buried regions underneath the source regions with higher body-dopant concentration. In carring out the processing steps to form these oxide spacers, a special anisotropic etching process, e.g., a reactive ion etching (RIE), process is performed which often leads to special problems and limitations in manufacturing the power device. Leakage of the junction currents, directly below the space edges is often reported in device formed with oxide spacer. The problems can be attributed to silicon loss and spacer etch damages in the substrate which also lead to defects formed in the subsequent source implant and anneal. The performance of the power device and the reliability are therefore adversely affected due to these difficulties when spacers are implemented which are formed with these processing steps. Another problem is related to the gate oxide integrity. After the buried body implant, the oxide spacer is removed with a wet etch for subsequent source implant. The wet etch process results in cavities at the edge of the polysilicon gate. The cavities are not refilled during subsequent source diffusion process due to the time of diffusion is not sufficient to cause enough growth of the silicon oxide to refill the cavities. For high density MOSFET device, the cavities on edges of the gate is a more sever problem because a very short source diffusion is usually carried out to avoid deep junctions when longer source diffusion is performed.

In spite of these difficulties, a designer is nevertheless faced with a constant challenge to increase the device ruggedness due to the fact that various internal parasitic components often impose design and performance limitations on a conventional power metal oxide silicon field effect transistor (MOSFET). Among these parasitic components in a MOSFET transistor, special care must be taken in dealing with a parasitic npn bipolar junction transistor (BJT) formed between the source, the body, and the drain. Under normal static conditions the base and emitter of the parasitic BJT are shorted, leaving only the body-drain diode effective. However, in a transient conditions and during an avalanche breakdown, the parasitic BJT may be activated incidentally which can seriously degrade the overall performance of the MOSFET. Under the circumstances when the parasitic bipolar junction transistor is incidentally activated, snap back may occur which can cause permanent damages to the device. For this reason, precaution must be taken to increase the ruggedness of the device by taking into account that an incidental activation of the parasitic BJT should be prevented in an avalanche breakdown condition when large amount of hole current is generated in the core cell area.

In order to better understand the design issues related to device ruggedness encountered in the prior art, general descriptions for the structure of a conventional power MOSFET device and design issues relating to device ruggedness are first discussed. FIG. **1** shows a typical vertical double diffused MOS (VDMOS) device which uses a double diffusion technique to control the channel length l. Two successive diffusions are performed with first a p diffusion using boron, then a n diffusion using either arsenic or phosphorus, to produce two closely spaced pn junctions at different depths below the silicon surface. With this pn junction, as shown in FIG. **1**, the VDMOS supports the drain voltage vertically in the n^{31} epitaxial layer. The current flows laterally from the source through the channel, parallel to the surface of the silicon. The current flow then turns through a right angle to flow vertically down through the drain epitaxial layer to the substrate and to the drain contact. The p-type "body" region in which the channel is formed when a sufficient positive voltage is applied to the gate. the channel length can be controlled through the processing steps. Because of the relative doping concentrations in the diffused p-channel region and the n– layer, the depletion layer which supports V_{DS}, a drain to source voltage, extends down into the epitaxial layer rather than laterally into the channel. Under the circumstances of avalanche breakdown, a hole current, i.e., I_h as shown in FIG. **1**, is generated to flow from the breakdown region to the source. A voltage drop, I_hR_b, is generated over the parasitic NPN bipolar junction transistor as the hole current I_h is transmitted via the p-body region underneath which has a p-body resistance R_b. When this voltage drop across this parasitic bipolar junction transistor reaches a certain level, e.g., 0.7 volts, the parasitic bipolar transistor is turned on. Activation of the parasitic bipolar transistor, as discussed above, could cause snap-back and permanent damages to the MOSFET device.

For the purpose of improving the device ruggedness, Motorola discloses in Electronic Engineering Times, Apr. 8, 1996, Page 78, a HDTMOS-2 structure. In that structure, after the n^+ source implant, a dielectric layer is grown on top of the polysilicon gate. The dielectric layer is etched to form the gate sidewall spacers for boron implant blocks, which are automatically self aligned with the source regions. This heavily doped p^+ region underneath the source region can reduced the body to source resistance R_b in the p-body region thus decreasing the voltage drop I_hR_b whereby the ruggedness of the MOSFET device is improved. However, additional difficulties arise from this spacer implementation. In order to fabricate the side-wall spacers, an anisotropic etch process is typically applied to remove the oxide in the flat areas while leaving the spacers at the side walls of the polysilicon gates. In order to account for variations in the spacer oxide layer thickness, some over etch is necessary. During the over-etch time, the field oxide and the silicon in the source or body junction regions may also be etched. Which may lead to the problems and difficulties discussed above. Furthermore, the uniformity of a reactive ion etch (RIE) process is difficult to control and the slope of the spacer may vary along the side-walls of the polysilicon gates. Which may then affect the self alignment and dopant profiles in subsequent ion implant operations to form the buried body-regions and the source regions. These difficulties in applying the RIE process cannot be easily resolved when the spacers are employed.

In order to reduce the body to source resistance, Korman et al. disclosed in U.S. Pat. No. 5,119,153 entitled "Small Cell Low Contact Resistance Rugged Power Field Effect Devices and Method of Fabrication" (issued on Jun. 2, 1992), a power field effect semiconductor device wherein an oxide or nitride spacer is used to form a heavily doped portion of a body region which is self aligned with respect to an aperture in the gate electrode. In forming the spacer, the nitride or oxide layer has to be formed and then anisotropically etched by reactive ion etching (RIE) in order to form the space along the side wall of the polysilicon silicon gate. Therefore, the device disclosed by Korman et al. is faced with the same technical difficulties associated with an-isotropic etching, such as an RIE process, as discussed above. Difficulties in manufacturability arising from imprecision of process control in applying this RIE method may also cause the cost of production to increase.

In yet another U.S. Pat. No. 5,268,586, entitled "Vertical Power MOS Device with Increased Ruggedness and Method of Fabrication", (issued on Dec. 7, 1993) Mukherjee et al. disclose a semiconductor device with improved ruggedness by forming a second body region, i.e., a second base region, within the first body region, under the source regions. As shown in a cross sectional view of FIG. **2**A, the second body region is shallower than the first body region and is formed close to the channel region to reduce the parasitic resistance in the first body region. The lateral edges of the second body region are substantially aligned with the lateral edges of the gate electrode. The first body region and the source region are formed by sequential implantation through the polysilicon gate electrode using the polysfficon gate electrode as a self aligned mask. The second body region is then formed by body implantation, again, using the polysfficon gate as the implant mask, without substantial lateral diffusion. Since the second body region is formed without substantial lateral diffusion, very limited thermal budget is allowed for the this second body region. Reduction of the drain to source resistance is quite limited because, without enough diffusion process, this second body region is formed with reduced depth under the source regions. Furthermore, high contact resistance between the metal and the body region may occur due to a low P+ surface doping concentration as the net dopant concentration as a function of depth along the line F-F' shown in FIG. **2**B. Additional difficulties of higher threshold voltage may also arise from lateral diffusion of the second body region to touch the channel region. Finally, a polysilicon layer of greater thickness employed in this structure may cause another problem. For high density DMOS device, poor metal coverage may occur when the re-firing of the thicker polysilicon layer to block the high energy body implant ions causes the contact openings to have high aspect ratio, i.e., high height to width ratio.

Therefore, there is still a need in the art of power device fabrication, particularly for power MOSFET design and fabrication, to provide a simplified and improved fabrication process that would resolve these limitations.

SUMMARY OF THE PRESENT INVENTION

It is therefore an object of the present invention to provide a new and novel MOSFET cell structure, and fabrication process to form the self aligned deep and shallow high-concentration body-dopant regions to improve the device ruggedness and to remove a top portion of the lightly doped source region to reduce the contact resistance whereby the aforementioned limitations encountered in the prior art can be overcome.

Specifically, it is an object of the present invention to provide a new and improved MOSFET manufacture process and cell structure by performing the shallow and deep p+ body implant operations after the contact opening process wherein the thick insulation layers covering the gates are employed as ion-blocks for body implants to form the self-aligned deep and shallow p+ body regions and followed by removing the lightly doped n+ surface portion as the result of doping compensation form the p+ body implants in the contact openings whereby the contact resistance is reduced.

Another object of the present invention is to provide a new and improved MOSFET manufacture process and cell structure by performing the shallow and deep p+ body implant operations after the contact opening process wherein the thick insulation layers covering the gates are employed as ion-blocks for body implants to form the self-aligned deep and shallow p+ body regions and a high energy ion implant to form the deep p+ body region is performed either without an implant oxide or with an implant angle less than seven degrees (7°), e.g., at zero degree, from a perpendicular direction to the substrate surface, in order to form a deeper channeling-enhanced high concentration body dopant profile in the body region to further improve the device ruggedness.

Another object of the present invention is to provide a new and improved MOSFET manufacture process and cell structure by performing the shallow and deep body implant operations after the contact opening process wherein the thick insulation layers covering the gates are employed as ion-blocks for body implants to form the self-aligned deep and shallow high concentration body regions whereby the requirement of additional masks or sidewall spacers as that employed in the prior art are no longer necessary and higher product quality and reliabffity can be achieved with this simplified manufacture process.

Another object of the present invention is to provide a new and improved MOSFET manufacture process and cell structure by performing the shallow and deep body implant operations after the contact opening process wherein the thick insulation layers covering the gates are employed as ion-blocks for body implants to form the self-aligned deep and shallow body regions wherein the p+ body-dopant regions are kept at a certain lateral distance away from the channel regions by taking advantage of the thickness of the insulation layers applied as ion blocks whereby the concerns of threshold voltage increase caused by lateral diffusion of the body dopant to the channel regions as that encountered in the prior art are eliminated.

Briefly, in a preferred embodiment, the present invention discloses an improved method for fabricating a MOSFET transistor on a substrate to improve a device ruggedness. The fabrication method includes the steps of: (a) forming an epi-layer of a first conductivity type as a drain region on the substrate and then growing an initial oxide layer over the epi-layer; (b) applying an active mask for etching the active layer to define an active area followed by depositing an overlaying polysilicon layer thereon and applying a polysilicon mask for etching the polysilicon layer to define a plurality of polysilicon gates; (c) removing the polysilicon mask and then carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions; (d) applying a source blocking mask for implanting a plurality of source regions in the body regions with ions of the first conductivity type followed by removing the source blocking mask and a source diffusion process; (e) forming an overlying insulation layer covering the MOSFET device followed by applying a contact mask to open a plurality of contact openings there-

through; (f) performing a low energy body-dopant implant and high energy body dopant implant to form a shallow high-concentration body dopant region and a deep high-concentration body dopant region followed by applying a high temperature process for densification of the insulation layer and for activating a diffusion of the deep and shallow body dopant regions wherein the deep high-concentration body-dopant regions are formed below the source regions and extends beyond the contact regions but are kept at lateral distance away from a channel region of the MOSFET device in the body region whereby the device ruggedness is improved without the concern of increasing the threshold voltage.

These and other objects and advantages of the present invention will no doubt become obvious to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment which is illustrated in the various drawing figures.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a cross-sectional view of a prior art structure of a general MOSFET;

FIGS. **2**A is a cross-sectional view of another prior art MOSFET structure with a heavily doped body region underneath the source implanted by using the gate as dopant blocks without diffusion and aligned substantial with the edges of the gate to improve the device ruggedness;

FIG. **2**B shows the variation of the net dopant concentration as a function of the depth along a line F-F' of the MOSFET of FIG. **2**A;

FIGS. **3**A to **3**D show the cross sectional views of the active area of a MOSFET transistor at different major stages for manufacturing a MOSFET device of the present invention with a high concentration shallow body region, and a deep heavily doped body-region formed underneath the source;

FIGS. **4**A to **4**F are a series of net dopant concentration profiles during different stages of the manufacturing processes;

FIGS. **5**A to **5**F show the detail processing steps of manufacturing the MOSFET device of this invention; and

FIG. **6** is a cross section view of a trenched MOSFET device of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to FIGS. **3**A to **3**D for the novel processing steps to manufacture a power MOSFET device to increase the device ruggedness and to reduce the contact resistance according to the present invention. Started from FIG. **3**A, the processing steps are described after the source diffusion process are completed to illustrate the major features of the present invention. More details for the manufacture processes will be discussed below in FIGS. **5**A to **5**E. Referring to FIG. **3**B, a first insulation layer **148** comprising preferably NSG or PSG insulation layer is formed. A second insulation layer **145** comprising preferably a BPSG insulation layer is formed over the top. A contact mask (not shown) is applied to open a plurality of contact openings **150** through the first and second insulation layers **145** and **148**. These contact openings **150** are applied here as the low energy and high energy high concentration body implant windows. A low energy implant body implant with boron or BF^2 is first carried out to form the shallow high concentration body region **160** near the top surface of the contact openings **150**. A high energy body implant with boron ions is performed to form the deep high concentration body region **165**. Referring to FIG. **3**C, a BPSG reflow is performed where the profile of the second insulation layer **145**, e.g., a BPSG layer, are changed to a smooth profile as shown. In the meantime, the elevated temperature applied to carry out the BPSG reflow also activate the diffusion of the shallow and deep high concentration body regions **160** and **165** respectively. Referring to FIG. **3**D, after the BPSG reflow process, a contact silicon etch is performed to remove a portion from the top surface of the contact openings. As shown in FIG. **3**D, the top portion removed has a depth of δ. After the top layer of thickness δ is removed, a layer of source contact metal **170** is formed over the top.

The advantages of the present invention can be appreciated by referring to the net dopant concentration profiles as shown in FIGS. **4**A to **4**F. In FIG. **4**A, a net dopant concentration along line A-A' of FIG. **3**A is shown. This net dopant concentration profile is a typical profile without having a deep high concentration body dopant region. Referring to FIG. **4**B, along the line B-B' in FIG. **3**C, a deep P+ region **165** (DP+) is formed. In the meantime, the source ion concentration at the top surface near point B is decreased. This is caused by the compensation of the implant of the shallow high concentration body region **160** which reduces the net source ion concentration near the top surface of the source regions **140**. Referring to FIGS. **4**C and **4**D along the lines C-C' and D-D' in FIG. **3**D. After the top layer of thickness δ is removed, the portion of the source region **140** which has lower net dopant concentration is removed. Thus the difficulty of higher contact resistance caused by a lower net source dopant concentration at the top surface due to the shallow p+ body implantation is removed. Referring to FIG. **4**D, the contact resistance in shallow p+ region **160** is also improved. Furthermore, the device ruggedness is improved with a deep P+ body region **165** formed underneath the source region **140**. FIGS. **4**E and **4**F are the net dopant concentration profiles along lines C-C' and D-D' respectively which are further improved when the deep body implant is carried out by taking advantage of a channeling effect by either skipping the process of growing a layer of implant oxide or by arranging an implant angle smaller than a regular implant angle of seven degrees, i.e., 7° relative to the perpendicular direction to a top surface of the substrate. It is a general industry practice to grow an implant oxide to prevent implant damage. As the activation temperature employed in this invention is kept at a relatively low level to avoid a stacking fault induced by a higher temperature during the activation process, thus the process of growing an implant oxide layer may be skipped to obtain the benefit of further improved device ruggedness with a channeling enhanced profile. By implanting either without an oxide layer or by implanting the deep high concentration body region with implant angle less than 7°, the body dopant ion can penetrate through a greater depth into the body region without being scattered by either the implant oxide or the particles in the lattice structure. The greater body dopant concentration beneath the deep body implant region **165** further improve the ruggedness of the device. Because this higher body dopant concentration deep down in the body region serve the purpose of further reducing the resistance in the lower body region. The likelihood of incidentally turning on the parasitic bipolar transistor due a voltage drop across that region is therefore further reduced.

Referring to FIGS. **5**A to **5**F for the processing steps employed to manufacture the MOSFET device of the present invention. The process begins by first growing a N

epitaxial layer **110** with a resistivity ranging from 0.1 to 1.0 ohm-cm on top of a N+ substrate **105**. The substrate has a resistivity of 0.001 to 0.007 ohm-cm. The thickness and the resistivity of the epitaidal layer **110** depend on the requirements for device on-resistance and breakdown voltage. In a preferred embodiment, the thickness of the epi-layer **110** is about six to eight microns (6–8 μm). An initial oxide layer **115** of thickness in the range of 5,000 to 10,000 Å is grown which is then etched by applying a mask to define the active areas. In FIG. **5**B, a gate oxidation process is first carried out to form a gate oxide layer **120**. A polysilicon layer **125** is then deposited on the gate oxide layer **120**. A $POCL_3$ doping process is carried out followed by an arsenic (As) implant process with an ion beam of energy at 60–80 Kev with a flux density of 5 to $8\times10^{15}/cm^2$. A polysilicon mask is then applied to carry out the an anisotropic etching process to define the polysilicon gate **125**. The resist is stripped and a p-body implant at 30–100 Kev with an ion beam of 3×10^{13} to $3\times10^{14}/cm^2$ flux density to form the p-body region **130**. A p-body diffusion process is then carried out at an elevated temperature of 1,000–1,200° C. for ten minutes to three hours to increase the depth of the p-body region **135** to 1.0–2.0 μm.

Referring to FIG. **5**C, a N+ block mask **135** is applied to carry out an N^+ implant to form the N^+ region **140**. The N^+ implantation is carried out with an ion beam at an energy of 60–100 Kev and ion flux density of 5×10^{15} to $1\times10^{16}/cm^2$. After the resist is stripped, the N+ source regions **140** are driven into desired junction depth ranging from 0.2 to 1.0 μ by a diffusion process. A NSG or PSG is deposited to form a first insulation layer **148** of approximately 1000–5,000 Å in thickness. A BPSG layer is deposited to form a second insulation layer **145** of about 5,000 to 15,000 Å in thickness. Referring to FIG. **5**D, a contact mask is applied to perform an etching process to define a plurality of contact windows **150**. A shallow body implant is performed to form a shallow high concentration body region **160** with either a low energy boron implant with an ion flux of 1×10^{14} to $2\times10^{15}/cm^2$ at about 20 to 60 Kev or a high energy BF_2 implant with an ion flux of $1\times10^{14}/cm^2$ to 2×10^{15} at about 100–240 Kev. Then a high energy body implant is carried out by either skipping a step of grwoing an implant oxide layer or implanting with an implant angle smaller than seven degree (7°), e.g., at zero degree relative to the perpendicular direction to the top surface of the substrate, to form a deep high concentration body region **165** with boron ions of an ion flux of about 3×10^{14} to $1\times10^{16}/cm^2$ at about 100 to 300 Kev. A region in the lower portion of the body region **130** with higher body dopant concentration is formed because of the channeling effect as that shown in FIGS. **4**E and **4**F. Further improvement of device ruggedness is achieved because of this channeling-body dopant region formed in a greater depth in the body region **130**.

Referring to FIG. **5**E, a BPSG reflow and densification process is performed at 900–950° C. for thirty minutes to one hour. The shallow body region **160** and the deep body region **165** are activated. An etch process is performed to remove a top portion of the silicon layer from the contact windows **150**. The thickness **6** of the top portion removed ranging from 300 to 3,000 Å. The contact resistance between the metal contact **170** and the source region **140** is reduced with the removal of this top portion because the low net source dopant concentration of the source region **140** at the top surface caused by body dopant implant compensation is now removed.

According to FIGS. **5**A to **5**E and above descriptions, this invention discloses a method for fabricating a MOSFET transistor on a substrate. The method includes the steps of (a) forming an epi-layer of a first conductivity type as a drain region in the substrate and then growing an initial oxide layer over the epi-layer; (b) applying an active mask for etching the active layer to define an active area followed by depositing an overlaying polysilicon layer thereon and applying a polysilicon mask for etching the polysilicon layer to define a plurality of polysilicon gates; (c) removing the polysilicon mask then carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions; (d) applying a source blocking mask for implanting a plurality of source regions in the body regions with ions of the first conductivity type followed by removing the source blocking mask and a source diffusion process; (e) forming an overlying insulation layer covering the MOSFET device followed by applying a contact mask to open a plurality of contact openings there-through; and (f) performing a low energy body-dopant implant and high energy body dopant implant to form a self-aligned shallow high concentration body dopant region and a self-aligned deep high concentration body dopant region. In a preferred embodiment, after forming the self-aligned shallow high concentration body-dopant region and the self-aligned deep high concentration body dopant region, the step (f) further includes a step of applying a high temperature process for densification of the insulation layer and for activating a diffusion of the deep and shallow high concentration body dopant regions. In a preferred embodiment, the method further includes a step (g) of applying an etching process for removing a top portion of the substrate from the contact openings for providing a source contact area of lower contact resistance. In a preferred embodiment, the step (f) of performing a high energy body dopant implant to form a self-aligned deep body dopant region is a step of applying a channeling-effect implant by performing the high energy body dopant implant without an implant oxide layer. In a preferred embodiment, the step (f) of performing a high energy body dopant implant to form a self-aligned deep body dopant region is a step of applying a channeling-effect implant by performing the high energy body dopant implant at an implant angle of less than seven degrees from a perpendicular direction to a top surface of the substrate. In a preferred embodiment, the step (f) of performing a high energy body dopant implant to form a self-aligned deep body dopant region is a step of applying a channeling-effect implant by performing the high energy body dopant implant at an implant angle of zero degrees from a perpendicular direction to a top surface of the substrate. In a preferred embodiment, the step (f) is a step of applying the channeling-effect implant by skipping an implant oxide layer formation process and by performing the high energy body dopant implant at an implant angle of seven degrees from a perpendicular direction to a top surface of the substrate.

Referring to FIG. **6** for a trenched MOSFET device **200** which is manufactured by a similar process as described above to have a shallow p+ region **260** and a deep p+ region **265** in the p-body region **230** formed in the substrate between the trenched gate **225**. The deep p+ region is formed beneath the source region **240** and are formed by a high energy body dopant implant through the contact openings between the first insulation layer **248** and the second insulation layer **245**. The deep p+ region **265** and the shallow p+ regions are formed as self aligned regions with the insulation layers **248** and **245** serving as body dopant implant blocks. Because of the thickness of these insulation layers, the deep body doped regions **265** are prevented from being laterally

diffused to contact the channels. There is no adverse effect to the threshold voltage caused by a contact of the deep p+ region with the channels because a greater distance of the deep body doped region is maintained with the first and second insulation layers **248** and **245** which block the body dopant ions to come dose to the channel regions next to the trenched gates **225** adjacent to the source regions **240**.

Therefore, the present invention provides a new and improved MOSFET cell structure, and fabrication process to form the self aligned deep and shallow high concentration body-dopant regions to improve the device ruggedness and to remove a top portion of the lightly doped source region to reduce the contact resistance whereby the limitations and difficulties of the prior art are resolved. Specifically, a new and improved MOSFET manufacture process and cell structure are disclosed wherein the shallow and deep body implant operations are performed after the contact opening process with the thick insulation layers covering the gates employed as ion-blocks for body implants to form the self-aligned deep and shallow high concentration body regions and followed by removing the lightly doped surface portion in the contact openings whereby the contact resistance is reduced. With the thick insulation layers covering the gates employed as ion-blocks for body implants to form the self-aligned deep and shallow high concentration body regions, the high energy ion implant to form the deep high concentration body region is performed either without an implant oxide layer or with an implant angle less than seven degrees (7°) whereby a channeling-enhanced body dopant profile at the lower portion of the body region is formed which further improve the device ruggedness. Since the shallow and deep body high concentration implant operations are performed after the contact opening process with the thick insulation layers covering the gates employed as ion-blocks for body implants, self-aligned deep and shallow body regions are formed without the requirements of additional masks or sidewall spacers as that employed in the prior art, and higher product quality and reliability can be achieved with this simplified manufacture process. Furthermore, the shallow and deep body implant operations are performed after the contact opening process with the thick insulation layers covering the gates employed as ion-blocks, the deep high concentration body-dopant regions are kept at a certain lateral distance away from the channel regions by taking advantage of the thickness of the insulation layers applied as ion blocks whereby the concerns of threshold voltage increase caused by lateral diffusion of the body dopant from the deep high concentration body dopant regions to the channel regions as that encountered in the prior art are eliminated.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is not to be interpreted as limiting. Various alternations and modifications will no doubt become apparent to those sdilled in the art after reading the above disclosure. Accordingly, it is intended that the appended claims be interpreted as covering all alternations and modifications as fall within the true spirit and scope of the invention.

We claim:

1. A method for fabricating a MOSFET transistor on a substrate comprising steps of:

a) forming an epi-layer of a first conductivity type as a drain region in said substrate and then growing an initial oxide layer over said epi-layer;

(b) applying an active mask for etching said active layer to define an active area followed by depositing an overlaying polysilicon layer thereon and applying a polysilicon mask for etching said polysilicon layer to define a plurality of polysilicon gates;

(c) removing said polysilicon mask then carrying out a body implant of a second conductivity type followed by performing a body diffusion for forming a plurality of body regions;

(d) applying a source blocking mask for implanting a plurality of source regions in said body regions with ions of said first conductivity type followed by removing said source blocking mask and a source diffusion process;

(e) forming an overlying insulation layer covering said MOSFET device followed by applying a contact mask to open a plurality of contact openings there-through; and

(f) performing a low energy body-dopant implant and high energy body dopant implant to form a self-aligned shallow high concentration body dopant region and a self-aligned deep high concentration body dopant region.

2. The method for fabricating said MOSFET transistor of claim **1** wherein:

after forming said self-aligned shallow high concentration body-dopant region and said self-aligned deep high concentration body-dopant region, said step (f) further includes a step of applying a high temperature process for densffication of said insulation layer and for activating a diffusion of said deep and shallow high concentration body dopant regions.

3. The method for fabricating said MOSFET transistor of claim **1** further comprising:

(g) applying an etching process for removing a top portion of said substrate from said contact openings for providing a source contact area of lower contact resistance.

4. The method for fabricating said MOSFET transistor of claim **1** wherein:

said step (f) of performing a high energy body dopant implant to form a self-aligned deep body dopant region is a step of applying a channeling-effect implant by performing said high energy body dopant implant without an implant oxide layer.

5. The method for fabricating said MOSFET transistor of claim **1** wherein:

said step (f) of performing a high energy body dopant implant to form a self-aligned deep body dopant region is a step of applying a channeling-effect implant by performing said high energy body dopant implant at an implant angle of less than seven degrees from a perpendicular direction to a top surface of said substrate.

6. The method for fabricating said MOSFET transistor of claim **5** wherein:

said step (f) of performing a high energy body dopant implant to form a self-aligned deep body dopant region is a step of applying a channeling-effect implant by performing said high energy body dopant implant at an implant angle of zero degrees from a perpendicular direction to a top surface of said substrate.

7. The method for fabricating said MOSFET transistor of claim **4** wherein:

said step (f) is a step of applying said channeling-effect implant by skipping an implant oxide layer formation process and by performing said high energy body dopant implant at an implant angle of seven degrees from a perpendicular direction to a top surface of said substrate.

* * * * *